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Design and Implementation of High Speed, Low Power LVDS Receiver Architecture in 18nm FINFET Process Technology

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Abstract: The Proposed work offers a novel LVDS (low-voltage differential signalling) receiver circuit design and implementation that is full adherence to the LVDS specification. The architecture is proposed to satisfy the needs of applications which requires fast data speeds and minimal power usage. This LVDS receiver architecture composed of Common mode compressor stage, amplification stage, Differential to Single Ended (D2S) and Buffer stages. The LVDS receiver Circuit simulations show that the receiver supports 5 Gbps data rate, 0.67 mA current at 0-2.4V input supply. With a power consumption of 1.2mW, the circuit aims to provide low power consumption and high data rate. The suggested circuit efficiency and validity are confirmed by achieving circuit simulation in 18 nm FinFET standard technology at 1.8V I/O (Input/Output interface) voltage. The LVDS has the benefit of supporting both low power and high-speed signalling. Furthermore, it is free from the severe under and overshoots that are a feature of high-speed rail-to-rail signalling standards. With greater input supply voltage ranges of 0 to 2.4 volts, this design is easily transportable to multiple application with different voltage levels. The proposed design exhibits rising-falling delays, P2P (Peak to Peak) rise-fall jitter in the transient simulation, also shows Gain in AC simulation results. The P2P Rise and fall jitter tabulated from Eye diagrams representation of output waveform for Typical, Slow, and Fast corners measured at different temperatures with respect common mode voltage range. Through AC modelling, a gain of 7.67dB is obtained at typical corner level with input voltage of 1.2V. For the suggested LVDS receiver architecture, additionally rise, fall delay characteristics were captured by Monte Carlo simulations for various common mode voltage ranges like 100 mV, 1.2V, and 2.3V. The layout of proposed LVDS architecture is designed by using desired layout techniques to achieve area optimization. Hence designed proposed LVDS receiver architecture supports the total area of 49µm*76µm.

Keywords: *LVDS, TIA/EIA-644, Receiver, Low power, High speed, FinFET.*

1.Introduction

LVDS is a high-speed data transmission, interface technology that was proposed in the 1990s and its receiving technology has the following characteristics such as low power consumption, minimal signal swing, fast transmission speed, and anti-interference [1]. Low voltage, low noise, low power and high-speed IO interfaces are the goals of LVDS development. It has good noise immunity and fast data transfer also lower power using a small swing differential signal of 350 mV. Differential data transmission transfers the data between two wires that have opposing voltage swings. When common mode noise is coupled across two wires, the receiver rejects because it only analyses the signal difference between the two. It emits less noise because the differential signal cancels the magnetic field, small swings also result in less power consumption [2]. Among differential cable driving standards like RS422 and RS485, LVDS has the least differential swing. Small bit error rate (BER), high speed, high resolution are important for a high-performance CIS (Computer information systems) system. Hence, LVDS technology is frequently utilised due to its exceptional noise and fast speed immunity to noise in the common mode [3]. A common standardised data transmission format for serial data transmission is called LVDS [4]. Different technologies, such as Current Mode Logic (CML), LVDS and Low-Voltage Positive-Emitter-Coupled Logic (LVPECL), have developed industrially interfaces with high signalling rates. Each standard has different power consumption and signalling rate capabilities [5]. As per the LVDS standard, the maximum voltage that can be applied to the LVDS receiver's input terminals is limited to 2.4V and should not be lower than 0V. Rail-to-rail OpAmps, on the other hand, are a crucial component of the LVDS receiver because conventional OpAmps are unable to achieve such a broad dynamic input range at low supply voltages (3.3V even lower) [8]. The ANSI standard defines LVDS [11], and its electrical requirements are listed in Table 1. Specifically, when compared to single-ended buffers, LVDS buffers provide the benefits of higher data rate, lower power usage, better common-mode noise rejection. Different receiver and driver designs that meet multiple needs are made possible by LVDS technology. The increasing need for higher speed has led to an increased focus on I/O interface research work. A LVDS connection may make it feasible, enabling I/O circuits to operate in GHz range.

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The LVDS specifications state that a receiver must function within a broad input common mode voltage range of 0.05–2.35 V. Consequently, in order to use the 1.8 V supply voltage, the receiver must first accomplish the common mode voltage conversion [13].

Table 1: Electrical Specifications of LVDS Standard.

Parameter	Description	Min.	Max.	Units
V_{OD}	Differential output voltage	247	454	mV
V_{OS}	Common mode offset	1.125	1.375	V
$\|\Delta V_{OD}\|$	Acceptable mismatch in V_{OD}		50	mV
$\|\Delta V_{OS}\|$	Acceptable mismatch in V_{OS}		50	mV
$V_{OS_{pp}}$	Offset voltage variation		150	mV
I_{SC}	Short circuit current		24	mA
V_{TH}	Receiver threshold		100	mV

2. Design of LVDS Receiver Architecture

The proposed LVDS Receiver architecture is shown in Figure.1. The recommended LVDS receiver architecture consists of three main parts, common mode compressor circuit, amplification stage, D2S stage. The input signals (PADP and PADM) are received through an amplifier stage across the LVDS input common-mode compressor circuit which supports voltage ranges of 0 to 2.4 V. A ESD block protects the IO circuit from ESD. Simultaneously, the output common mode Vcm from common mode compressor circuit applied to analog inverter stage which act as amplification stage. In this design self-biasing is achieved, it helps to burn extra current, save lot of area, leakage power and dynamic power. The proposed architecture provides a low power and high-speed solution for LVDS receivers to support different application with variable voltage ranges. The proposed LVDS Receiver architecture schematic block diagram of every internal component is discussed in Figure 2. From the Figure.2 the input signal PADP and PADM are passed though ESD protection circuit without any signal changes then Common mode compressor circuit converts from common mode voltage range of 0-2.4V in to PDK supported signal range 0-1.8V, then signal get amplified by amplification stage. The Level shifter is used here to convert the voltage levels and D2S helps to transfer the differential output to a single-ended output, Finally VOUTP, VOUTN acts as output signals from the LVDS receiver architecture.

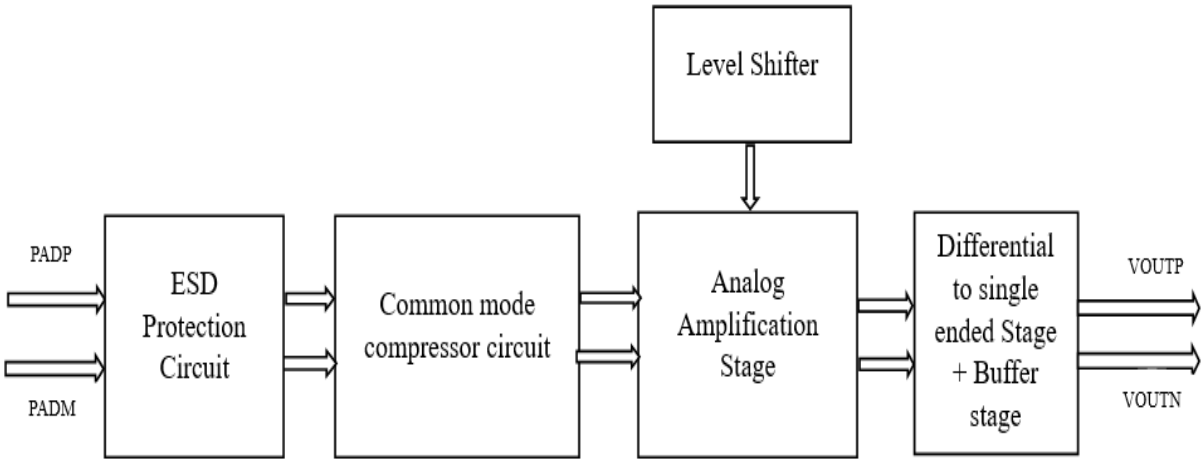

Fig 1. Block diagram of LVDS receiver

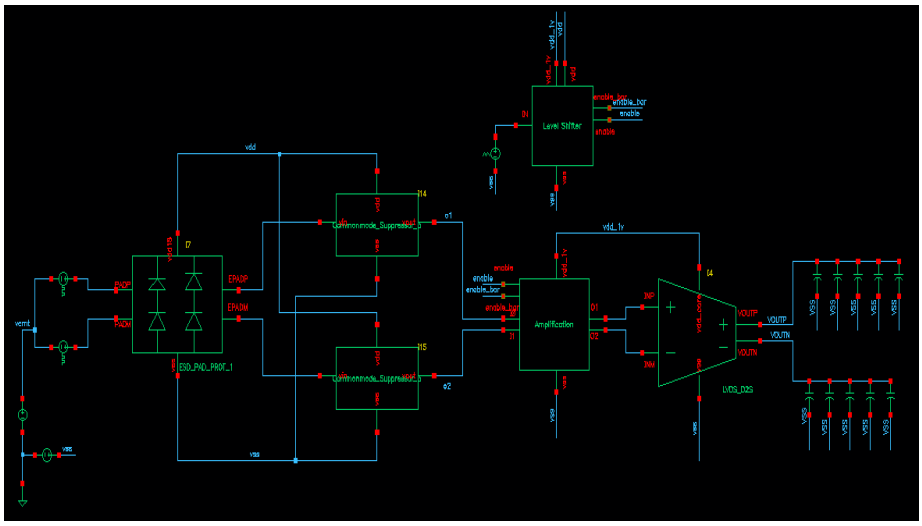

Fig 2. Schematic representation of LVDS receiver architecture

2.1 ESD protection circuit

Device Protection against Electro Static Discharge (ESD), usually located near to the I/O interface pad. Mitigating the negative effects of ESD events is the goal of I/0 placement. Diodes that function under forward-biased conditions and are seamlessly incorporated into integrated circuit designs are a popular option for ESD protection equipment. However, ESD protection diodes, especially large-diameter ones, have parasitic effects that can impact high-frequency circuit operational efficiency. Eliminating the parasitic capacitance connected to ESD protection diodes becomes essential to achieving this. The article offers a brief solution in response, consisting of two unique I/O pads that combine an ESD protection diode and stacked passive devices arrangement designed for K/Ka-band applications. This novel method implementing to reduce signal loss and improve ESD protection. On silicon chips, a contrast of the suggested and traditional I/O pad designs with ESD protection has been performed. The experimental results verify the feasibility of the suggested structures, which maintain ESD-protection effectiveness with less signal attenuation than the conventional design. These results feature the suggested approach can serve for high-frequency applications, also highlighting the significance of thoughtful ESD protection strategies while simultaneously enhancing signal integrity. Figure.3 shows the ESD circuit used in proposed LVDS architecture.

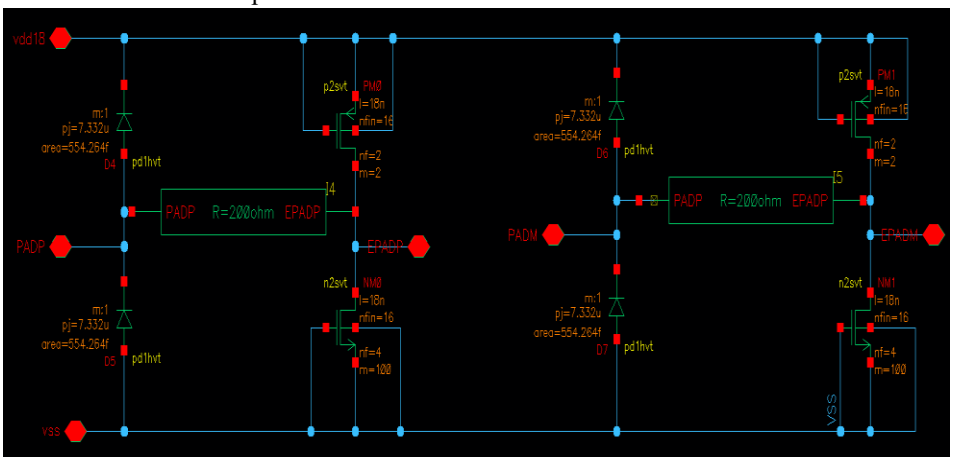

Fig 3. Schematic diagram of ESD protection Circuit

2.2 Common mode compressor circuit

For an LVDS receiver to operate in compliance with LVDS specifications, a broad input common mode voltage range of 0.05-2.35V is necessary. Because of this, the receiver needs to use the 1.8V supply voltage to finish the common mode voltage conversion first. A simple common mode voltage suppressor circuit consisting of a resistor and capacitor as shown in Figure.4. This circuit measures the common mode voltage difference between the input data PADP and PADM, amplifies it by applying or removing current from resistors R0 and R1 in order to activate the current regulator. The resistors R0, R1 experience voltage dips, VDD18 adjusts the common mode voltage as a result. By adjusting the VREF voltage to 0.9V, a amplification with a higher gain is produced. Merely 1.8V devices can be utilised for this design by employing the current PDK. In order to prevent device

malfunctions caused by unreliability, common mode must be suppressed. Therefore, to prevent reliability issues, use a suppressor circuit that converts voltage range from 0 to 2.4 volts to 0 to 1.8 volts. The suggested receiver supports wide range common mode, allowing the same IP to be used at 5 Gbps speed for an unlimited number of applications. The output voltage range of this proposed compressor circuit will be between 0.7 and 1.2 volts, with the common mode input being given as 0 to 2.4 volts. As a result, there are no dependability problems with the devices and they are safe because lower voltages prevent device degradation. The amplifier circuit's capacitive load functions as an LPF when the compressor circuit output is fed to the gate voltage of circuit. Low pass filters (LPFs) are a class of filters that block high-frequency signal while allowing low-frequency ones to flow through. LPF only permits lower frequencies to reach the output after the cutoff frequency has reduced. To prevent a pole at RC in the compressor circuit, capacitor C2 is connected in parallel to resistor R2. Zero introduced to ensure that gain falloff does not occur, Gain fall off should occur at a higher frequency rather than at or below the operating frequency because the pole at the RC roll off will cause the gain to fall off early in the circuit design.

The compressor circuit resistor equivalent values can be expressed as (1) and (2),

$$\frac{\left(\frac{R_1R_2}{R_1+R_2}\right)*1.8}{\left(\frac{R_1R_2}{R_1+R_2}\right)+R_0} = 700\ \text{mV}$$ When input =0V Output =700mV……..(1)

and

$$\frac{\left(\frac{R_1R_2*1.8}{(R_2+R_1)}\right)}{\left(\frac{R_1R_2}{(R_2+R_1)}\right)} + \frac{\frac{R_0}{R_0R_1}}{\frac{R_0R_1}{R_0+R_1}+R_2} = 1.2\ \text{V}$$ When input =2.3V output=1.2V……..(2)

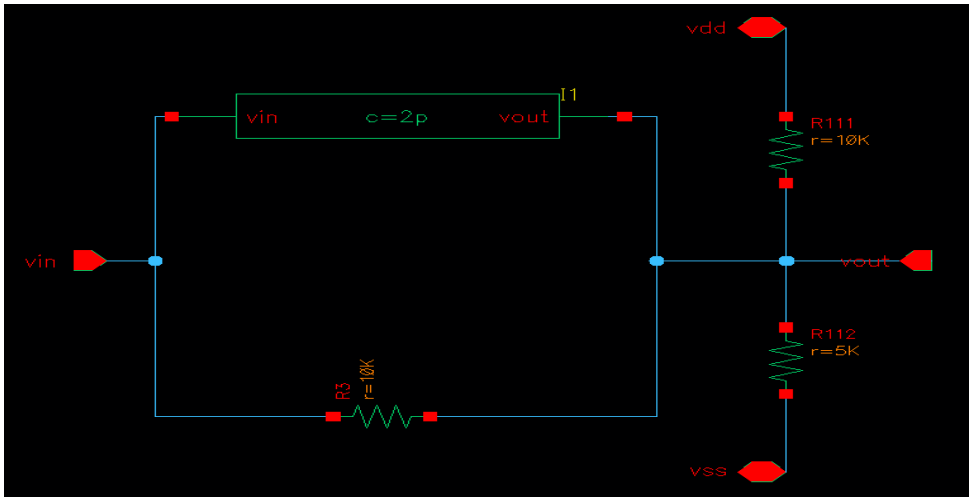

Fig 4. Schematic diagram of Common mode Compressor Circuit

2.3 Analog Amplifier Stage

To achieve Higher speed and power consumption as low as possible analog amplifier stage is used to work as amplification stage. The output voltage ranges of 0.7V to 1.2V from common mode compressor circuit is applied as input voltages to analog amplifier stage. In both analogue and digital circuits, inverters are incredibly helpful electronic components. Figure.5 shows an analog inverter condition with a feedback resistor (Rf) is connected between the transistor drains and transistor grids in linear applications. The transistor pair's stable operating point is thus found. Now when input is rising, the output is falling but Rf will ensure input and output points are stable at DC level. Whatever supply voltage (1.8V) parameter β ratio of pmos and nmos are same and Ron of pmos and nmos are same. Hence when supply voltage is 1.8 V, the output voltage of analog inverter is 0.9V. Rf will ensure the output and input of inverter hold at some value with respect to DC point. The same stable point decided by Ron of pmos and nmos as Ron of pmos and nmos same here so the output voltage value go to half of the supply voltage called DC point. When small input swing of 100mV applied to analog inverter stage around 0.9V amplification will happen and that will get amplified to 1V. Also, this inverter stage will give sufficient gain from 100mV to almost 1V. For two ideal complementary transistors the transition from high (VDD) to low output level occurs at a common input voltage of VDD/2. The midpoint of this "quasi-linear" transition region also at VDD/2. Therefore, a feedback resistor Rf between output and common input creates the correct bias. However, when the common input node is connected (via a capacitor) to a signal voltage the feedback resistor Rf also acts as a load resistor. Since the MOS transistor pair acts as a current source, the load resistor determines the voltage gain of the whole circuit.

The gain of analog inverter circuit expressed as,

Gain=(gmp=gmn)(rop=ron=R)
……..(3)

Also, Bandwidth of analog inverter expressed as

F=1/(2πRload.Cout)……
……....(4)

where

Rout=(rop=ron=R)andCout=((cddp+cddn+cload)
……..(5)

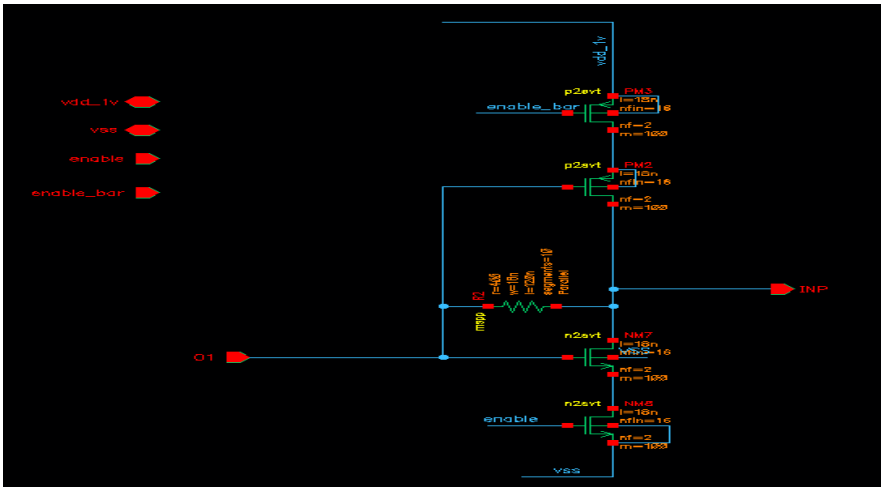

Fig 5 Schematic diagram of Analog amplifier circuit

2.4 Level Shifter Circuit

The traditional level shifter, which employs a cross-coupled PMOS load shown in Figure. 6. The NM11, NM12, PM18, and PM19 were designed to withstand high voltage stress using a thick gate oxide transistor. NM11 and NM12's gate source voltage provides nodes T1 and T2 with latching voltage. In cross-coupled systems, this voltage is used. Node T1's VddH voltage is fully generated by the positive feedback action of PM18 and PM19. In cases where VA is low, Two of the three are turned on: NM11 and NM12, and PM18 and PM19. Upon switching to high at that point, if VA process is carried out. T1 switches from low to high, PM18 is turned off, and NM11, NM12, and PM1 are turned on. Ultimately, the PM1's current driving capability determines the time it takes the voltage to change from low to high. As the output changes states before the pull-down nmos can defeat the PMOS latch action, NM11 and NM12 are significantly larger than PM18 and PM19.

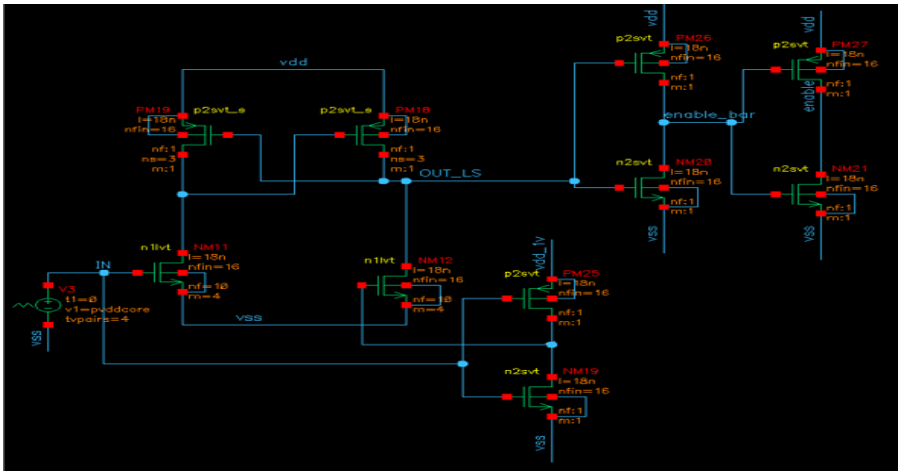

Fig 6: Schematic diagram of Level shifter Circuit

2.5 Differential to Single Ended Circuit and Buffer stage

The LVDS receiver uses a D2S stage as seen in Figure.7, to transfer the differential output to a single-ended output. The amplifier circuit receives the swing multiplied by two at the output after conversion from the receiver circuit, which uses a PADP, PADM with a differential swing of 100 mV to +100 mV on the input side. This double swing, which is not rail to rail (sig2p and sig2n), is fed into the differential to single-ended circuit. The D2S circuit will transfer the signal from differential to single-ended because of its dual swing. The number of swings required is increased by D2S in order to convert the analogue signal

into a CMOS signal, then CMOS signal passed to the buffer stage to create a rail-to-rail waveform. The buffer stage of NMOS devices amplifies the signal to provide higher capacitive loads after the first stage of D2S. In D2S stage the input signals INP and INM are differential, and gm*INP represents the D2S output.

The Gain(G) of the D2S stage circuit is represented as

$$G = gm(NM1) * r_0(NM1) \quad \ldots\ldots (6)$$

parallelwithr0(PM7). After receiving rail-to-rail signal, the inverter chain will double the differential swing, making it almost rail-to-rail, and avoid it. The D2S circuit does not use a resistive load; only a Mosfet load is used. The buffer stage determines the strength of the signal which is needed to drive large loads shown in Figure. 7.

The final outputs OUTP and OUTN are rail-to-rail CMOS signals, is produced by the LVDS receiver using the inputs vols and volsn .

The output Vols is defined in D2S as

$$Vols = V_{in} * G \quad \ldots\ldots (7)$$

$$Vols = (INP - INM) * G \quad \ldots\ldots (8)$$

where, Vin -differential input

The output of the amplification stage serves as the D2S's input,

$$INP = fun(G1 + G2 + G3) * (PadP - PadN) \quad \ldots\ldots (9)$$

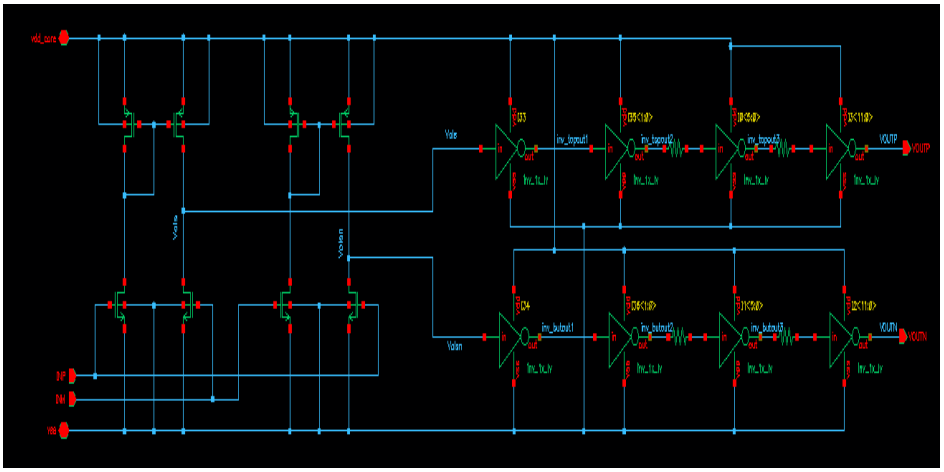

Fig 7. Schematic diagram of D2S Block with Buffer stage

Basic inverter stages are responsible for improving the strength of the signal needed to drive larger loads, they are based on D2S stages. The LVDS receiver generates the final output, a rail-to-rail CMOS signal, using the inputs vols and volsn and the outputs VOUTP and VOUTN. Figure.8 illustrates the addition of a Flywheel inverter with signal names inv_butout1, inv_butout2, and inv_butout3 after each inverter stage. The inverter stage in this circuit is to provide an exact 180°C phase shift when complimentary signals are present. To achieve this, the switching point must be precisely at vdd/2.

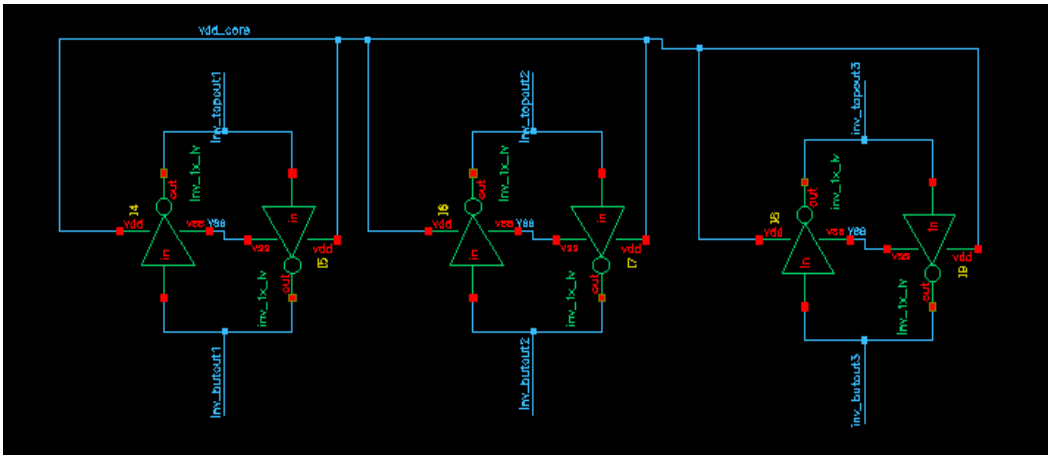

Fig 8. Schematic diagram of Flywheel Circuit

3. Experimental Results and Discussion

The proposed LVDS receiver is constructed and analysed in part 2. A 100Ff capacitor connected to the LVDS receiver design for pre-simulation. As stated in this Results section, the three corners Typical, Slow, fast with different high- and low-frequency ranges were analysed using transient analysis for large signals and AC analysis for small signals. Vcm represents the common mode voltage ranges from 0-2.4V, here in result section Vcm =1.2V considered to tabulate all parameters and waveforms.

3.1 Transient Analysis of LVDS Receiver

In the transient simulation depicted in Figure.9, the LVDS receiver amplifies a 100mV low-dropout signal to a 0–2.4 V full-scale signal in accordance with the IEEE LVDS standard. The transient analysis waveforms of Figure.9 show the input signals PADP, PADM of the receiver circuit and the output signals VOUTP, VOUTN, which indicate an amplified 1V output signal. Table 2 contains a tabulation of the various process corners, such as Typical -TT(C0), Slow Slow-SS (C1, C2), and Fast Fast -FF (C3, C4) simulation results. The following temperature ranges are considered with regard to distinct corners: 27°C, -40°C and 125°C. The circuit uses a load capacitance 100 fF, an input signal frequency of 2.5GHz, and an input signal swing of 100 mV. Table 2 lists the peak-to-peak jitter results for the rise and fall at 1.8 V power supply voltage, as well as the rise and fall delays. Peak-to-peak jitter of the proposed LVDS receiver circuit estimated by an eye diagram simulation. Figure.10 illustrate how the 5Gbps LVDS signal of the intended receiver was used to replicate the output eye diagram at the typical corner at 27°C. For a standard corner at 27°C, the eye diagram, as shown in Figure.10, calculated the output signal's peak-to-peak rise and fall jitter to be 4.33 ps and 4.495 ps, respectively.

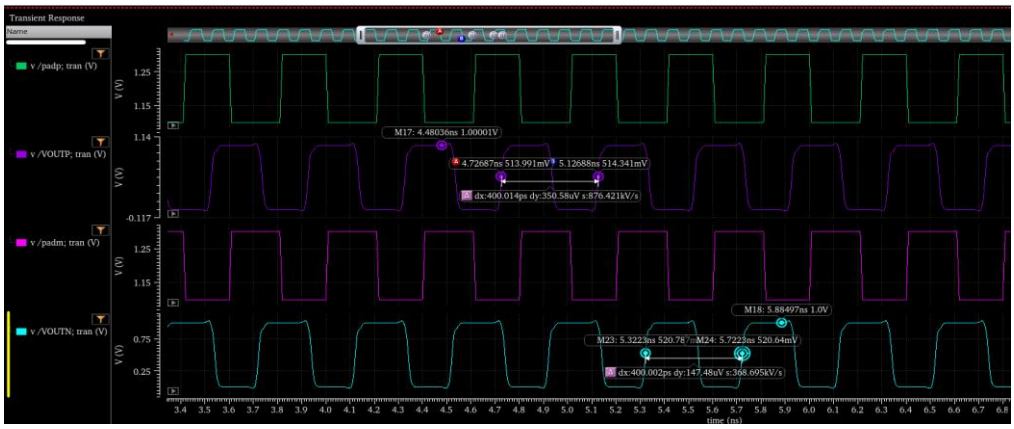

Fig 9. Transient simulation of LVDS receiver at Vcm=1.2V

Table 2: Transient Analysis of LVDS Receiver at Vcm=1.2V

Parameters	**C0**	**C1**	**C2**	**C3**	**C4**
Temperature	27℃	-40℃	125℃	-40℃	125℃
Frequency	2.5 GHz	2.5 GHz	2.5 GHz	2.5 GHz	2.5 GHz
pvdd18	1.8V	1.72 V	1.88 V	1.72 V	1.88 V
Rise Delay	103.401ps	116.16ps	154.38ps	77.31ps	105.12ps
Fall Delay	130.25ps	149.057ps	192.65ps	95.085	128.026ps
IO_Power	1.208mW	589.6uW	1.463mW	1.096mW	3.106mW
P2P Rise Jitter	4.340 ps	7.776 ps	7.528 ps	2.060 ps	1.270 ps
P2PFall_Jitter	4.495 ps	7.378 ps	7.013 ps	2.632 ps	2.312 ps

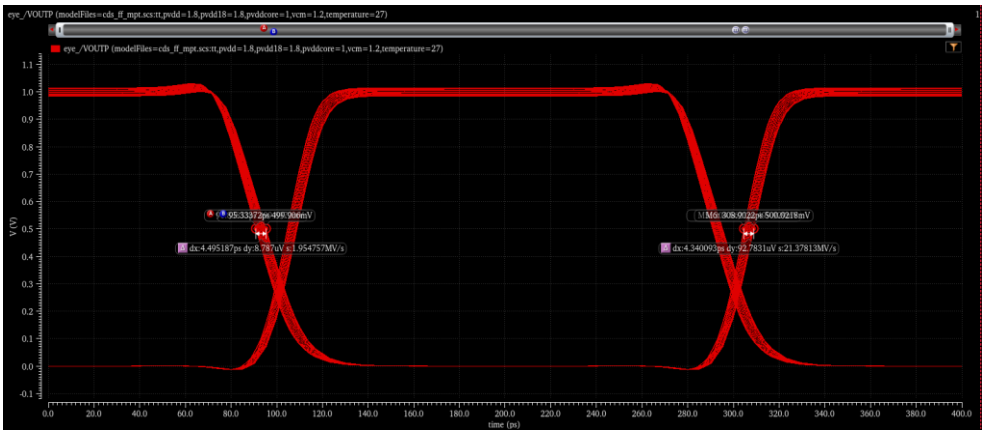

Fig 10. Eye Diagram of LVDS Receiver at Typical Corner C0: 27°C at Vcm=1.2V

3.2 AC Analysis of LVDS Receiver

Figure.11 shows the frequency, amplitude, and gain characteristics of the LVDS receiver. The LVDS receiver's low-frequency gain and unity-gain bandwidth are shown in the simulation at different process corners and temperatures.

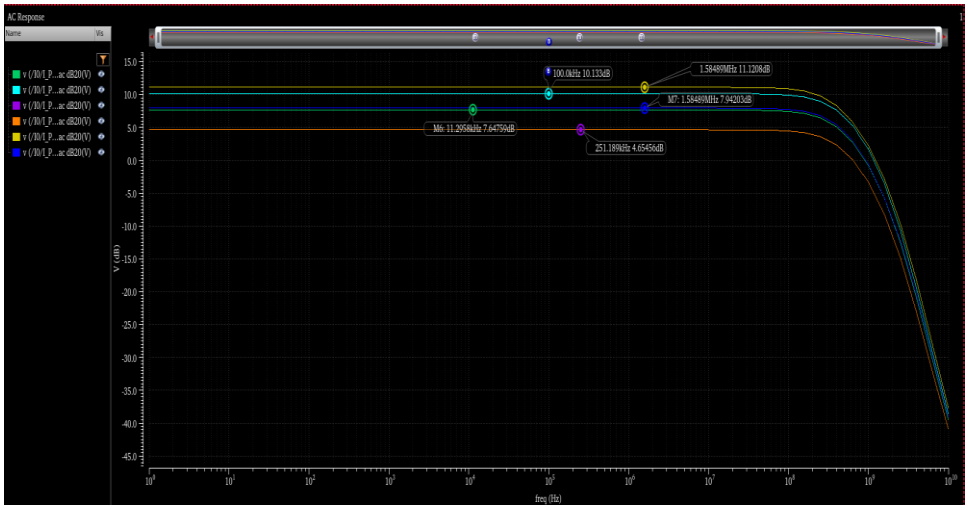

Fig 11. AC simulation of LVDS receiver at Vcm=1.2V

Table 3 explains in detail that the C0 corner has frequency of 2.5GHz and gain of 7.647 dB at at Vcm=1.2V. The low-frequency gain at the C1, C2 corners is 10.133 dB at -40 °C and 4.654 dB at 125 °C, respectively. Similarly, the low-frequency gain at the C3, C4 corners is 11.120 dB at -40 °C and 7.942 dB at 125 °C, respectively.

Table 3. Gain of Amplification stage at Vcm=1.2v

Parameters	**C0**	**C1**	**C2**	**C3**	**C4**
Temperature	27°C	-40°C	125°C	-40°C	125°C
pvdd18	1.8V	1.72V	1.72V	1.88V	1.88V
Gain	7.647dB	10.133 dB	4.654 dB	11.120 dB	7.942 dB

3.3 Monte Carlo Analysis

As technology advances, it becomes increasingly important to analyse the process variation of the circuits because device dimensions are decreasing. Monte Carlo simulations are used to verify that this suggested work is more robust than the current designs against changes in local and global processes. Table 4 display the output of the Monte Carlo simulation for the power, and delay distribution of the suggested LVDS receiver. The bell-shaped normal distribution will be the shape of the frequencies of the different outcomes generated by this simulation. The graphs in Figure.12 and Figure.13 show the rise and fall delay distribution of the proposed design as found by Monte Carlo simulation, respectively.

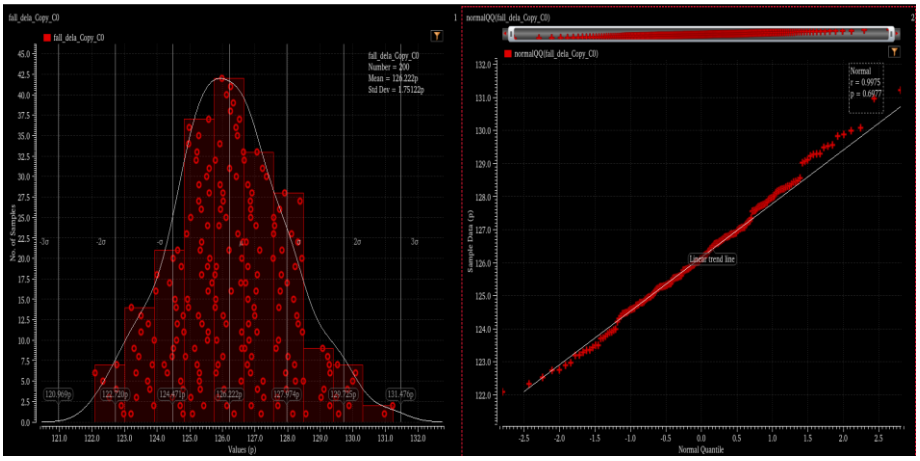

Fig 12: Fall delay distribution of Montecarlo simulation results at Vcm=1.2V

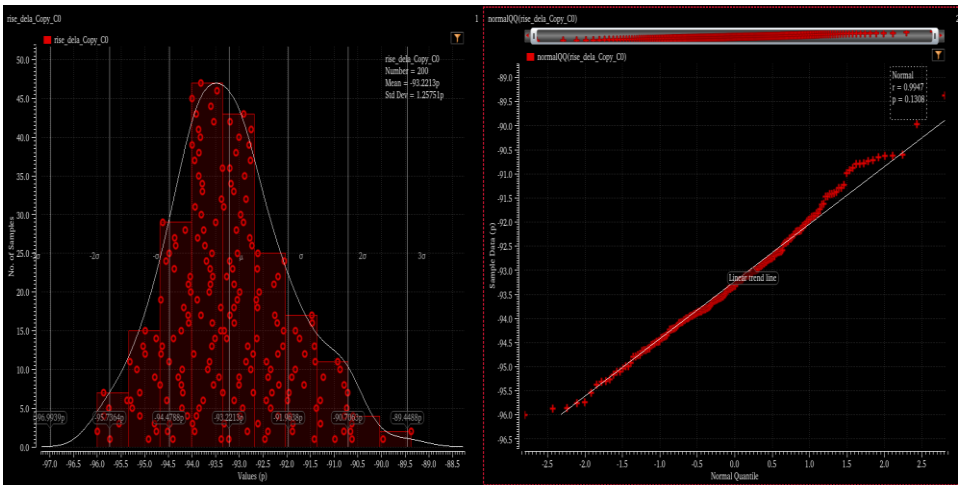

Fig 13: Rise delay distribution of Montecarlo simulation results at Vcm=1.2V

Table 4: Monte Carlo Analysis of Proposed LVDS Receiver at Vcm=1.2v

Name	Std Dev=1 Sigma	Mean-3Sigma	Mean	Mean+3Sigma
Rise_Delay_CO(ps)	1.258p	89.446p	93.22p	96.994p
Fall_Delay_CO(ps)	1.751p	120.947p	126.2p	131.453p
IO_Power_CO	56.81u	1.03957m	1.21m	1.38043m
Core_Power_CO	700.4u	41.4288m	43.53m	45.6312m

Table 5 shows a comparison with some of the published literature that is most relevant to this topic and summarises the simulated performance of the proposed LVDS receiver. The suggested FINIFET 18nm-based LVDS architecture has a higher data rate of 5 Gbps and a proportionate power of 1.2mW at a typical corner temperature of 27°C when compared to earlier research. Therefore, high-speed applications may be able to use this LVDS architecture. The Cadence Virtuoso tool is used to implement this work with FINFET 18nm technology.

Table 5. Performance Comparison with proposed work outcomes.

Parameters	[1]	[2]	[3]	[4]	Proposed Work
Process	180nm CMOS	180nm CMOS	180nm CMOS	28nm CMOS	18nm FINFET
Frequency	500MHz	1.2GHz	2.68 GHz	500 MHz	2.5GHz
Voltage	1.8 V	3.3 V	2.5 V	1.8 V	1.8 V

Power	326 mW	2.4 mW	10.5 mW	0.2 mW	1.2 mW
Capacitive Load	1pF	12 pF	-	-	100fF
Data rate	500 MS/s	1.2 Gbps	1.2 Gbps	1Gbps	5Gbps
Area	49*22µm	0.464 mm2	0.067 mm2	0.009mm2	49*76um

3.4 Physical Design of Proposed LVDS Receiver

The proposed circuit layout for 18nm FINFET process is depicted in Figure .14. the layout using the 18 nm standard FINFET process. The dimensions of the layout area are 49 µm by 76 µm. respectively, while the cell area is only 3724um2. When compared to the works shown, this cell's power consumption is also advantageous. The current implementation satisfies all TIA-644-A electrical specifications and can tolerate supply variations between 0V and 2.4V domains. The shielding effect, symmetrical phases of the differential signal lines, and matching of the input differential pair transistors are the main factors taken into account in the layout design of the LVDS receiver. Guard ring is used for protection of devices in ESD blocks and single ended buffer stages. Two types of matching technique are used in single ended buffer. For PMOS devices used "Inter-digitization" matching Technique as it is a current mirror circuit. For NMOS devices used "Common centroid" matching Technique as it is a differential amplifier circuit. By using symmetrical design and compact layout design techniques, the total area of the circuit is reduced, and the metal parasitic resistance and capacitance were minimized.

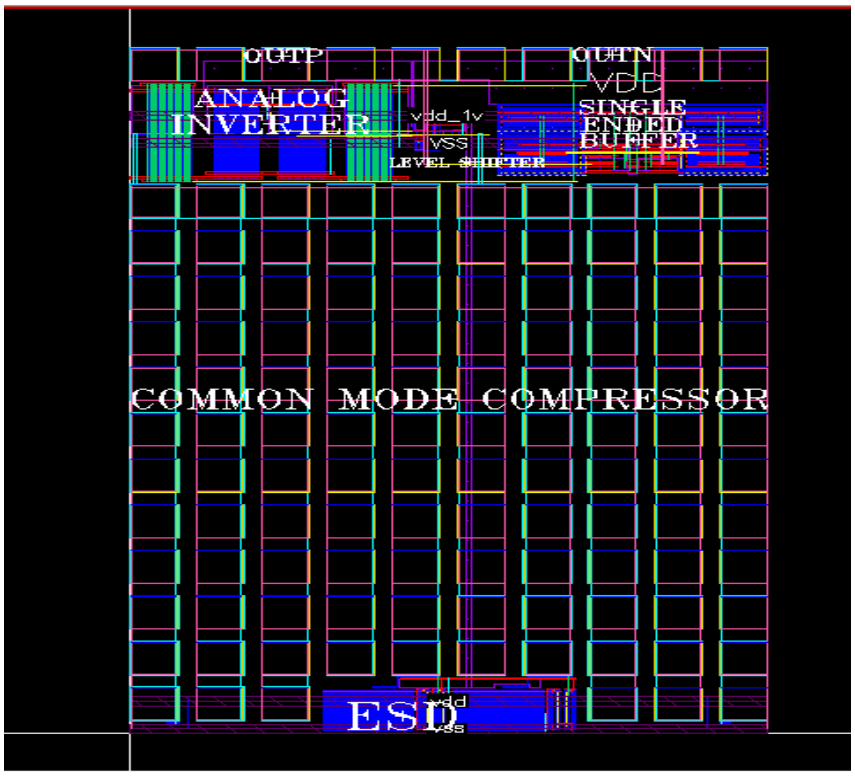

Fig 14: Layout Design of LVDS Receiver architecture

4. Conclusions

This proposed work depicts the design of a self-biased LVDS receiver circuit using an 18 nm FINFET process. The LVDS receiver design includes an amplification structure and a self-biasing circuit. The output signal is converted from differential to single-ended after comparison. The range of signal reception is increased by the LVDS receiver through self-adjustment of the bias. The designed circuit was subjected to transient and AC circuit simulation. The receiver's transient simulation and AC simulation results are compliant with the LVDS standard. The layout area of the LVDS receiver is 49µm*76µm, and the output signals P2P jitter is approximately 4.3ps in Typical corner at Vcm equal to 1.2V. The proposed architecture provides power consumption about 1.2mW at 1.8 V voltage and 5Gbps data rate. The comparison results with the related works shows that the proposed LVDS receiver architecture supports high data rate, low power and common wide

voltage range. Hence this LVDS receiver architecture compatible to work with multiple high-speed applications. The focus of future work also can target to achieve high speed, low power, optimised area of LVDS receiver architecture that can support common mode ranges with more programmability features.

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