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Optimized Full Swing Gate Diffusion Input Logic in Low Power Design

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Abstract: Power, delay and area optimized design techniques are consistently on high demand in semiconductor industry. Optimization techniques at system, architecture, gate and transistor levels are explored by researchers to combat the requirements of low power chips needed for industries. Grain level optimizations at gate and transistor levels offers higher reduction in power when compared with system and architectural levels. This paper focuses on optimization of Gate diffusion Input technique, a gate level approach for low power. This research presents the fact that Full Swing Gate Diffusion Input technique offers power, delay and area efficient circuits only for Boolean functions realized with a greater number of complemented literals rather than functions with true literals. This finding was verified by the implementation of Boolean functions exclusively comprising of true literals and complementary literals. The results depicted that Full Swing Gate Diffusion Input implementation is suitable only for Boolean functions comprising of complementary literals. For functions with true literals, the equations have to be modified to exploit the benefits of Full Swing Gate Diffusion Input techniques. The implementation was extended to realization of the state of the art 1-bit full adder, using conventional CMOS, direct FSGDI and modified FSGDI. On comparison with conventional CMOS full adder, modified FSGDI with more complementary literals presented a significant 86% reduction in Power Delay Product when compared with direct FSGDI full adder that presented 23% reduction. Maximum reduction of power in FSGDI circuits can be realized when the circuits are modified for implementation with complementary literals.

Keywords: *GDI, FSGDI, Low power, Boolean, VLSI, Minimum Energy operation Point*

Introduction

Efficient design of VLSI circuits depends on its design topology. Traditionally, various circuit topologies such as CMOS, pass transistor gate logic, transmission gate logic and dynamic design were proposed. Each of these topologies has their unique advantages and drawbacks. Comparatively, CMOS design dominated semiconductor industry, owing to low power and simplicity in design. Alternatively, Gate Diffusion Input (GDI) [1-2] circuit topology offered drastic reduction in power when compared with traditional CMOS design and other topologies. Energy efficient quantum based GDI designs [3] have marked a significant insight in semiconductor industry. Consequently, improvements such as modified GDI [4], Full swing GDI (FSGDI) [5] and GDI with self-resetting logic [6] were developed. Basic GDI contributes to significant reduction in power. However, cascading multiple GDI stages leads to low output swing. The NMOS and PMOS transistors in GDI topology do not pull up and pull down effectively. This produces degraded outputs. To overcome the drawback of low outputswing, FSGDI was proposed [5]. FSGDI, shown in Fig. 1, produced full swing at the output, at the expense of increased number of inverters. Enhanced GDI technique [7] also presented only 0.01% reduction in power when compared to to GDI and CMOS. Hence, the fundamental idea of ultra-power reduction is compromised in FSGDI circuits. In the dimension of increased speed, a high-speed error tolerant full adder using GDI was proposed [8]. Optimized GDI method for reversible computation using genetic algorithm was implemented [9]. GDI based Scalable 1-bit hybrid full adder[10] and GDI based CSLA architectures[11] for high performance applications were proposed. GDI based approximate full adders[12] and GDI based imprecise subtractors[13], using CNTFET technology were proposed. Reversible full adder using dynamic GDI technique was presented [14]. Low power and low area digital modulators[15] using GDI was implemented. Approximate compressors using GDI have been designed for error tolerant applications[16]. Cyclic combinational GDI[17], switching patterns based GDI implementation[18], GDI based SRAM memory cells and multiple-valued logic gates using GDI[19] were the various application areas of GDI logic. GDI coupled with CNTFET transistors [20-23] were implemented to attain full swing in GDI circuits. GDI based Vedic multiplier [24-25], implemented at transistor level used only true literals to exploit

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the advantages of GDI. Hybrid approach of GDI based full adder design [26] was adopted to counterfeit the noise margin issues when full adder with complementary literals was implemented directly. GDI circuits based hardware security applications [27] has been proposed.

This research presents a detailed observation that limits the FSGDI approach in low power VLSI. An analysis of varied combinational expressions using FSGDI depicted that FSGDI circuits offered reduction in power, delay and area only for Boolean functions with Complemented Literals (CL). This inference will be highly useful for researchers to select designs that are suitable to be implemented with FSGDI topology.

In Section II, Boolean functions with True Literals (TL) and CL are independently implemented using FSGDI and CMOS, which proves that Boolean functions with CL are feasible to be implemented with FSGDI technique. In contrast, Boolean functions with complete TL are not feasible for FSGDI technique implementation. Section III illustrates the technique of converting Boolean function with complete TL to a function containing more CL, suitable for FSGDI implementation. Section III discusses the application of the technique in detail through state of art example of Full Adder (FA).

1 Materials and Methods

1.1 Experiment 1 - FSGDI and CMOS realizations of Boolean functions with true and complemented literals

Table I contains the Boolean functions that consist of true and complemented literals, which are necessary for conducting the experiment. The purpose of the experiment is to determine the applicability of FSGDI circuits in the context of low power design.

Table 1: Boolean functions with True and Complemented Literals.

Variables	Boolean Function	
	TL	CL
2	$F_{2a} = AB$	$G_{2a} = \overline{A}\,\overline{B}$
	$F_{2b} = A + B$	$G_{2b} = \overline{A+B}$
3	$F_{3a} = ABC$	$G_{3a} = \overline{A}\,\overline{B}\,\overline{C}$
	$F_{3b} = AB + C$	$G_{3b} = \overline{A}\,\overline{B} + \overline{C}$
	$F_{3c} = A + B + C$	$G_{3c} = \overline{A} + \overline{B} + \overline{C}$
	$F_{3d} = AB + BC + CA$	$G_{3d} = \overline{A}\,\overline{B} + \overline{C}\,\overline{B} + \overline{A}\,\overline{C}$
4	$F_{4a} = A + B + C + D$	$G_{4a} = \overline{A} + \overline{B} + \overline{C} + \overline{D}$
	$F_{4b} = AB + CD$	$G_{4b} = \overline{A}\,\overline{B} + \overline{C}\,\overline{D}$
	$F_{4c} = AB + CD + BD + AD$	$G_{4c} = \overline{A}\,\overline{B} + \overline{C}\,\overline{D} + \overline{B}\,\overline{D} + \overline{A}\,\overline{D}$

Traditionally, FSGDI circuits are implemented using Shannon's theorem [1]. For the purpose of design analysis discussion, the circuits F3d and G3d are considered. The design of FSGDI for F3d and G3d can be expressed through equations 1 and 2.

$$
\begin{aligned}
F_{3d} &= AB + BC + CA \\
&= A.F(1,B,C) + \overline{A}.F(0,B,C) \\
&= A.(B + C) + \overline{A}.(BC) \\
&= A.\{B.F(1,C) + \overline{B}.F(0,C)\} \\
&\quad + \overline{A}.\{B.F(1,C) + \overline{B}.F(0,C)\} \\
&= A.\{B.1 + \overline{B}.C\} + \overline{A}.\{B.C + \overline{B}.0\} \qquad (1)
\end{aligned}
$$

$$
\begin{aligned}
G_{3d} &= \overline{A}\,\overline{B} + \overline{B}\,\overline{C} + \overline{C}\,\overline{A} \\
&= A.F(1,B,C) + \overline{A}.F(0,B,C) \\
&= A.(\overline{B}.\overline{C}) + \overline{A}.(\overline{B} + \overline{C}) \\
&= A.\{B.0 + \overline{B}.\overline{C}\} + \overline{A}.\{\overline{B}.1 + B.\overline{C}\} \qquad (2)
\end{aligned}
$$

Figures 1 and 2 illustrate the representation of Equations 1 and 2, respectively, using FSGDI circuitry.

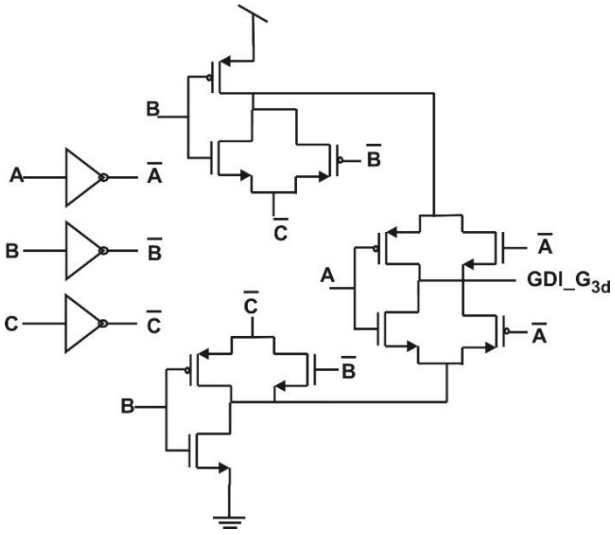

Fig 1: FSGDI realization of G3d

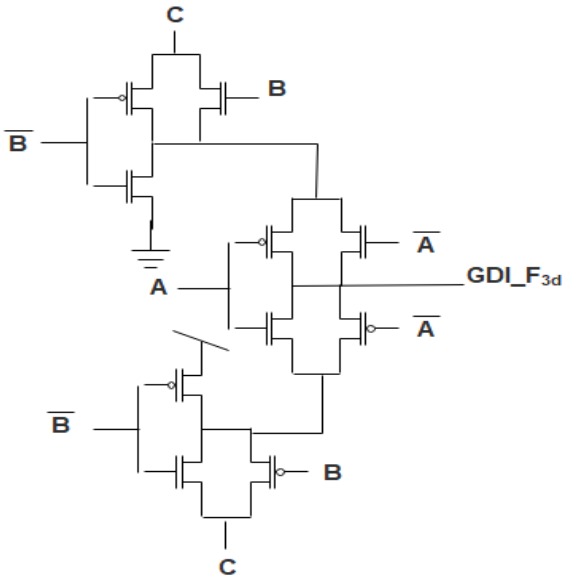

Fig 2: FSGDI realization of F3d

The identical design procedure is applied to all other Boolean functions listed in Table I. The outcomes of this experiment are elaborated upon in the Results and Discussion section. The outcomes explicitly indicate that, for the implementation of Boolean functions utilizing true literals, CMOS realization offers greater advantages compared to FSGDI implementation. Unlike FSGDI circuits, CMOS implementation circuits with true literals do not necessitate complemented inputs. However, when implementing Boolean functions with complemented literals, FSGDI realization proves more advantageous than conventional CMOS, as both CMOS and FSGDI implementations require inverters. Conventional GDI designs are executed with the assumption of accessible true and complemented inputs. Nonetheless, during the real-time implementation of FSGDI circuits, the inclusion of complemented inputs demands additional logic, leading to increased area and power consumption. Therefore, in this paper, we propose a FSGDI design methodology that calls for the modification of Boolean functions to reduce the count of complemented literals. To illustrate this point, we conduct Experiment 2 on a 1-bit full adder.

1.2 Experiment 2 - Proposed optimized algorithm for implementation of FSGDI circuits implemented on full adder

The proposed algorithm to identify the suitable architecture for implementation of FSGDI logic is illustrated as Algorithm 1.

Proposed Algorithm 1 for implementation of GDI circuits

Step 1	Identify the Boolean functions needed to realize the VLSI architecture A $\{B_1, B_2, \ldots \ldots B_n\} \subseteq A$
Step 2	For i in 1 to n
	Check if each B_i comprises of completely true literals or complemented literals
Step 3	If B_i comprises of at least one complementary literal for all true literals, the Boolean function can be implemented with FSGDI
Step 4	If B_i does not comprise of a complementary literal for all true literals, direct FSGDI is not suitable
Step 5	If Step 4 is true, identify alternative representation of Boolean function, that comprises of complementary literals.
Step 6	Implement the modified Boolean function using FSGDI

The state-of-the-art 1-bit full adder circuit is realized using three different styles: conventional CMOS, direct FSGDI, and the modified FSGDI implementation. This exemplary case serves to demonstrate the efficiency of FSGDI utilizing CL. The standard equation for a one-bit full adder is represented by equations (3) and (4).

$$Sum = A \oplus B \oplus C_{in} \quad (3)$$

$$Carry = AB + BC_{in} + AC_{in} \quad (4)$$

The proposed algorithm 1 for implementation of GDI circuits is applied on Boolean functions of 1-bit Full adder.

Proposed Algorithm 1 implemented on 1-bit Full adder

Step 1	:To realize the 1 bit Full Adder architecture A,the Boolean functions needed are
	{B_1,B_2 }={Sum,Carry}⊆A
Step 2	For i in 1 to 2
	Check if each B_i comprises of completely true literals or complemented literals
Step 3	B2 does not comprise of a complementary literal for all true literals. Hence, direct FSGDI is not suitable
Step 4	If B_i does not comprise of a complementary literal for all true literals, direct FSGDI is not suitable
Step 5	Since Step 4 is true,identify alternative representation for Carry that comprises of complementary literals.
Step 6	Implement the modified Carry function using FSGDI

Both FSGDI and CMOS topologies demand both the true and complemented variants of inputs for the implementation of the sum defined in equation (3). As a result, the sum can be effectively realized using FSGDI rather than CMOS. On the other hand, the carry expression in equation (4) is solely composed of true literals (TL), which means that direct FSGDI implementation would require extra inverters compared to its CMOS counterpart. To address this, equation (4) should undergo modification to take on a form that involves complementary literals (CL).

By applying Shannon's theorem, the direct FSGDI representation of Equation (4) is illustrated in Equation (5).

$$Carry = A.\{B.1 + \bar{B}.C_{in}\} + \bar{A}.\{B.C_{in} + \bar{B}.0\} \quad (5)$$

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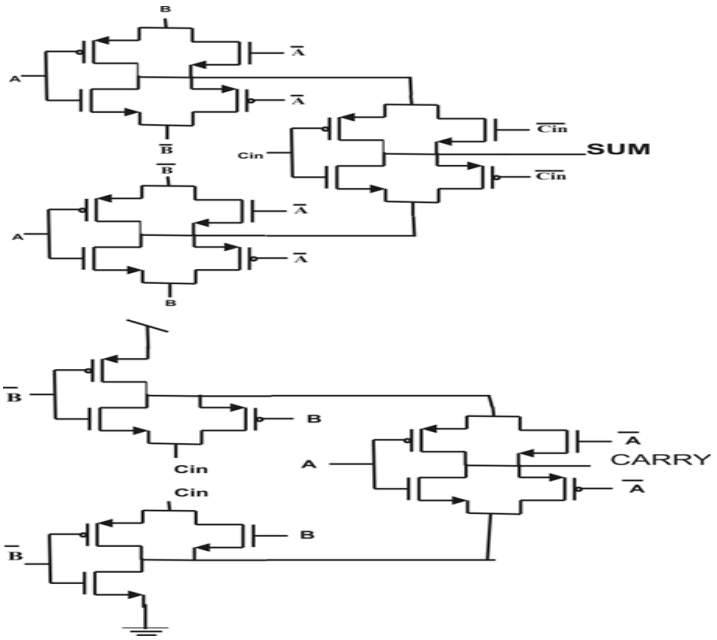

Fig 5. Direct FSGDI implementation of Full Adder

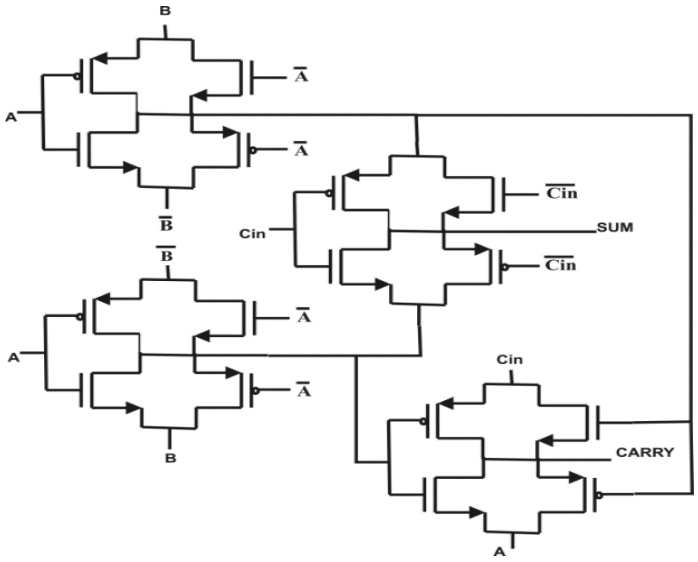

Fig 6. Modified FSGDI implementation of Full Adder

2 Results and Discussion

In this section of the manuscript, we present the results obtained from the implementation of Experiments 1 and 2, laying the foundation for subsequent deliberation. The evaluation of the experimental designs' centers on pivotal performance metrics, encompassing power consumption, delay, and area utilization.

2.1 Results and discussions of experiment 1

A comprehensive juxtaposition of FSGDI and CMOS designs in terms of area analysis is meticulously expounded upon in Table II and visually depicted in Figure 7. The quantities of transistors and inverters exhibit a direct and discernible relationship with the resultant design's area and power consumption characteristics.

Table 2: Analysis of number of transistors and inverters required for implementation of Boolean functions with true literals and distinct complemented literals.

VARIABLE COUNT	BOOLEAN FUNCTION	NUMBER OF TRANSISTORS		NUMBER OF INVERTERS	
		FSGDI	CMOS	FSGDI	CMOS
2	F_{2a}	5	6	1	1
	F_{2b}	5	6	1	1
	G_{2a}	8	9	2	3
	G_{2b}	8	9	2	3

3	F_{3a}	10	8	2	1
	F_{3b}	11	8	2	1
	F_{3c}	10	8	2	1
	F_{3d}	14	12	2	1
	G_{3a}	12	14	3	4
	G_{3b}	13	13	3	4
	G_{3c}	12	13	3	4
	G_{3d}	16	19	3	4
4	F_{4a}	15	10	3	1
	F_{4b}	16	10	3	1
	F_{4c}	19	15	3	1
	G_{4a}	17	18	4	5

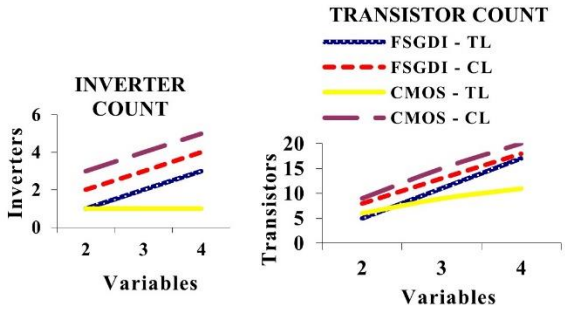

Figure 7. Analysis of number of transistors and inverters required for implementation of Boolean functions for True and Complemented literals.

Figure 7 illustrates a notable disparity between the FSGDI and CMOS realizations of CL, as evidenced by the markedly reduced count of transistors and inverters required by the former. In contrast, the FSGDI implementation of Boolean functions with TL demands a relatively higher count of transistors and inverters compared to its CMOS counterpart. These designs underwent simulation within a 180nm CMOS process, utilizing a supply voltage of 1 Volt. The Power Delay Product (PDP), recognized as the optimized performance benchmark for low-power designs, takes precedence in our analysis. Tables 3, 4, and 5 present a comprehensive overview of the Power, Delay, and PDP pertaining to Boolean functions featuring both true and complemented literals.

Table 3: Power analysis of FSGDI and CMOS realizations of Boolean functions.

VARIABLE COUNT	BOOLEAN FUNCTION	Power (microwatts)			
		FSGDI		CMOS	
TL_2V	F2a	0.89	1.045	1.12	1.06
	F2b	1.2		1	
TL_3V	F3a	2.01	2.232	1.26	1.03
	F3b	2.17		1.02	
	F3c	2.43		0.93	
	F3d	2.32		0.92	
TL_4V	F4a	3.57	3.39	1.01	0.86
	F4b	3.28		0.74	
	F4c	3.32		0.84	
CL_2V	G2a	1.93	2.015	3.06	2.795
	G2b	2.1		2.53	
CL_3V	G3a	2.89	3.06	3.91	3.502
	G3b	3		3.34	
	G3c	3.2		3.5	
	G3d	3.18		3.26	
CL_4V	G4a	4.45	4.28	4.52	4.49

	G4b	4.17		4.39	
	G4c	4.23		4.56	

Table 4: Delay analysis of FSGDI and CMOS realizations of Boolean functions.

VARIABLE COUNT	BOOLEAN FUNCTION	Delay (ps)			
		FSGDI		CMOS	
TL_2V	F2a	33.71	30.84	55.98	56.02
	F2b	27.97		56.06	
TL_3V	F3a	33.16	38.34	30.43	46.36
	F3b	28.21		49.42	
	F3c	28.11		51.97	
	F3d	25.55		53.66	
TL_4V	F4a	63.42	45.67	32.81	48.15
	F4b	37.09		55.42	
	F4c	36.52		56.23	
CL_2V	G2a	39.15	36.33	56.20	59.06
	G2b	33.52		61.93	
CL_3V	G3a	34.24	23.86	60.79	62.84
	G3b	37.81		61.20	
	G3c	7.62		60.87	
	G3d	15.79		68.53	
CL_4V	G4a	33.88	31.89	59.73	51.16
	G4b	31.33		47.52	
	G4c	30.46		46.23	

Table 5: PDP analysis of FSGDI and CMOS realizations of Boolean functions.

Variables	PDP (10^{-18} Watts sec)	
	FSGDI	CMOS
TL_2V	32.23	59.38
TL_3V	85.57	47.75
TL_4V	154.82	41.40
CL_2V	73.20	165.07
CL_3V	73.01	220.06
CL_4V	136.48	229.70

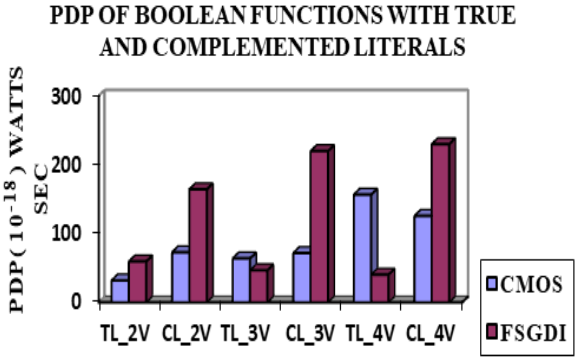

Fig 8: Analysis of Power Delay Product (PDP) for implementation of Boolean functions for True and Complemented literals in FSGDI and CMOS topologies.

Figure 8 effectively illustrates a substantial trend: the Power Delay Product (PDP) of FSGDI-realized CL Boolean functions, possessing two, three, and four variables, is significantly diminished by 55.55%, 67.33%, and 45.45%, respectively, in comparison to their corresponding CMOS counterparts. However, a contrasting pattern emerges for the PDP of FSGDI-realized TL Boolean functions of three and four variables, where an increase of 37.01% and an impressive 286.67%, respectively, is observed compared to their equivalent CMOS versions. This discernible escalation in PDP is predominantly attributed to the amplified count of inverters necessitated by the FSGDI implementation of TL, as elucidated in Figure 3. Consequently, the suitability of FSGDI for the implementation of Boolean functions with TL becomes distinctly questionable.

Operating at a low voltage is a pivotal factor in the realm of low-power design. Within this context, the determination of the Minimum Energy Point (MEP) assumes a notable role, particularly in the sub-threshold region of transistors [28]. Both TL and CL Boolean functions are subjected to reduced operational voltages to ascertain their respective MEPs. The cumulative energy consumption, denoted as Etotal, is effectively partitioned into dynamic (Edynamic) and static (Estatic) components. The specifics of the estimated MEP for both CL and TL Boolean expressions are meticulously presented in Table 6.

Table 6: Estimation of Minimum energy operation for CL and TL expressions

VOLTAGE	MEP (fJ)			
	TL		CL	
	F3c	F4a	G3c	G4a
0.10	0.523	0.552	0.562	0.532
0.14	0.501	0.423	0.521	0.452
0.18	0.312	0.275	0.422	0.321
0.22	0.210	0.362	0.381	0.452
0.26	0.332	0.412	0.324	0.521
0.30	0.382	0.523	0.265	0.586
0.34	0.412	0.621	0.121	0.621
0.38	0.521	0.698	0.321	0.712
0.42	0.623	0.721	0.456	0.825
0.46	0.712	0.795	0.652	0.868
0.50	0.798	0.825	0.851	0.912
0.54	0.852	0.910	0.898	0.941
0.58	0.912	0.978	0.912	0.998

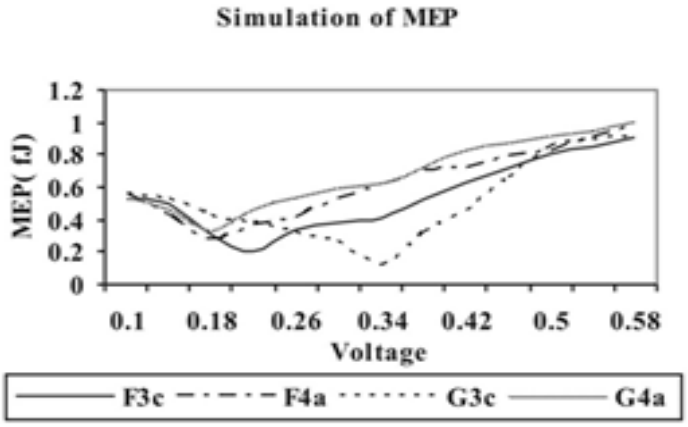

Fig 9: Minimum Energy Operation- Performance analysis

Figure 9 serves as a visual representation, revealing a significant observation: the Minimum Energy Point (MEP) for CL functions, namely G3c and G4a, exhibits a marked propensity for minimization in comparison to their corresponding TL functions, denoted as F3c and F4a. This scrutiny into performance, encompassing power, delay, and MEP, substantiates a key assertion: the adoption of the FSGDI topology for circuit design necessitates a meticulous evaluation of the Boolean functions integral to the design. Particularly, for sections of the designs where the prevalence of TL-based functions surpasses that of CL-based functions, strategic consideration should be given to exploring alternative design topologies or adapting the Boolean functions themselves. Such proactive measures

are essential to harness the full spectrum of low-power benefits of FSGDI circuits.

2.2 Results and discussions of experiment 2

A comparative analysis is undertaken between the modified version of the FSGDI full adder (FA), the original Direct FSGDI configuration, and the conventional 28T CMOS full adder. The outcomes of this comparison are succinctly consolidated in Table 7.

Table 7: Comparison of performance metrics of Full adders

Design	Transistor count	Power (µW)	Delay (ps)	PDP (fW)
Conventional CMOS FA	28	6.53	1048.7	6.848
Direct FSGDI FA	26	9.01	605.68	5.457
Modified FSGDI FA	20	4.62	137.05	0.633

From Table 7, it is evident that the Direct FSGDI FA has 20.33% decrease in PDP when compared to conventional static CMOS FA. Conversely, the Modified FSGDI FA, comprising of complementary literals exhibited 86% decrease in PDP when compared to conventional CMOS FA.

Figure 9 presents the variations in Power, Delay and PDP of the varied versions of full adders, for loads varying from 1fF to 91fF. It is observed that the power for direct FSGDI implementation of FA is much higher when compared to its CMOS version. In contrast, the modified FSGDI version of FA, with complementary literals exhibits the least power, delay and PDP.

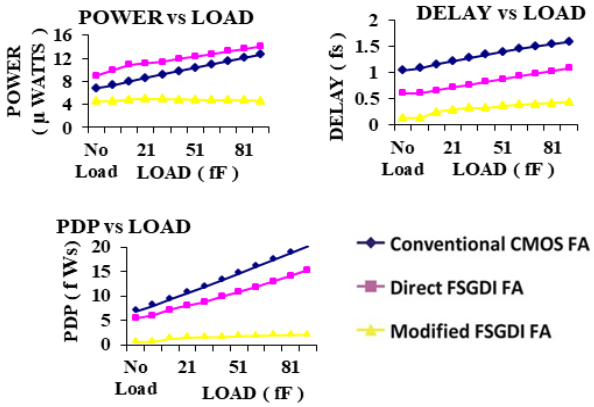

Fig. 9 Analysis of Power, Delay and PDP for full adders

Conclusions

FSGDI implementation has limitations in low power design. Varied Boolean functions with TL and CL were taken for analysis. The outcomes demonstrated that FSGDI realization of designs which involve more CL than TL exhibited significant power, delay and area advantages when compared to FSGDI realization of Boolean functions with TL. The state of art design such as FA was taken for analysis. The conventional form of FA, whose carry output involved true literals was not suitable for FSGDI implementation. Hence, a modified version of FA that contains more complemented literals was implemented using FSGDI. This research presents the scope of FSGDI in low power design methodologies, thereby specifying the conditions under which FSGDI is not beneficial. In such cases, the designer needs to alter the architecture of the design to make it suitable for FSGDI implementation.

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