International Journal of
INTELLIGENT SYSTEMS AND APPLICATIONS IN ENGINEERING
ISSN:2147-6799 www.ijisae.org Original Research Paper

Pseudo-Differential Tow-Thomas Biquad Architecture based Low Power and Low Area Analog Filter for 5G Applications

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Submitted:10/03/2024 **Revised**: 25/04/2024 **Accepted**: 02/05/2024

Abstract: Analog filters are used in huge number of integrated circuit designs such as radio frequency transceivers, global system for mobiles and wireless applications. The development of low power analog filter is a challenging task for communication applications, especially 5G communications. In this paper, a Pseudo-Differential Tow-Thomas Biquad (PDTTB) architecture for analog filter is proposed in Complementary Metal Oxide Semiconductor (CMOS) 45 nm technology for minimizing the size of transistors. The buffer incorporated in the designed PDTTB based low power and low area Analog Filter namely PDTTB-AF is used to avoid the degradation of signal in filter output. The High Voltage Threshold (HVT) transistor is developed in ring oscillator for minimizing the power consumption. The HVT transistor in analog filter has less subthreshold currents and reduces the leakage current. Moreover, the phase detector and charge pump are also designed with less number of transistors where HVT is used to minimize the power consumption in the filter. The main objective of this proposed architecture is to minimize the power consumption by using the less number of transistors which helps to develop area efficient filter. The proposed architecture is evaluated with area, delay, frequency, power and Figure-of-Merit (FoM). The existing research namely Low Voltage Mixed Mode (LVMM)-AF is used to evaluate the performances of PDTTB-AF architecture. The power consumption of PDTTB-AF architecture is 61.16uW which is lesser than that of LVMM-AF.

Keywords: *Analog filter, Complementary metal oxide semiconductor, High voltage threshold transistor, Pseudo-differential Tow-Thomas Biquad architecture, Power consumption.*

1. Introduction

A filter is generally a frequency-selective system that is utilized for altering input signal and filtering out the irrelevant signals to help in processing the input. Generally, the filters are classified into two types namely, analog and digital [1, 2]. The input and output variables are autonomously chosen as current or voltage for analog filter [3]. The analog filters functioning in transadmittance and/or transimpedance are used in different applications such as current mode, and/or voltage mode circuit is connected with the voltage mode and/or current mode architecture [4, 5]. Analog filters are essential building blocks and are utilized in continuous-time signal processing applications. Some of the applications are control systems, instrumentation, measurement and communication systems [6]. Examples of tasks which are carried out by analog filters are impedance matching in power amplifiers, frequency duplexing in radio communication and radar, and suppression of lower-sideband & upper-sideband in downconversion and upconversion mixers [7]. The oscillator is designed in different ways such as ring, relaxation circuit and inductor capacitor (LC) tank. The ring oscillator receives high attention because of the higher integration capacity and frequency tuning range in Voltage-Controlled Oscillator (VCO) design [8, 9].

Ring oscillator is extensively utilized in wired and wireless communication applications. Moreover, the ring oscillator is commonly an adopted block in phase locked loops utilized in RF and microprocessors. A higher tuning range, less power & area and ease of integration are permitting the utilization of ring oscillator in the fields of synchronization, data recovery and frequency synthesis [10, 11]. In that, Differential Ring Oscillator (DRO) has improved performances by means of supply noise and substrate because of the high common mode rejection ratio. The requirement of extra inverter is eliminated by providing both the true and complementary forms using DRO [12, 13]. More specifically, the square wave generation of ring oscillators mainly depends on the delay in the ring [14]. The technology of Complementary Metal Oxide Semiconductor (CMOS) is leading in recent times, permitting the Very Large-Scale Integration (VLSI) of complex circuits in a single chip. The advantages of VLSI circuits are evident; however, the growing complexity of electronic systems and components requires simple and low-cost fault testing for ensuring the precise operation. However, the accomplishment of the aforementioned tasks is complex and time consuming for the chips which have huge amount of transistors [15].

The contributions of the work are concise as follows:

- An analog filter is designed with Pseudo-Differential

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Tow-Thomas Biquad (PDTTB) in 45nm CMOS technology for decreasing the overall size. Its incorporation in the analog filter is used to eliminate the degradation in filtering process.

- The High Voltage Threshold (HVT) transistor is used to design the Ring Oscillator (RO) which minimizes the power consumption by minimizing the leakage current. The RO's oscillation frequency is easily tuned by altering the size of individual inverters that leads to develop the filter with modifiable cutoff frequencies. The simpler architecture of RO helps to minimize the area and power consumption. Additionally, the HVT transistor reduces the standby and dynamic power consumption without affecting the circuit performance.
- Additionally, the phase detector and charge pump are used in the PDTTB-AF is designed by using less number of transistors which further helps to minimize the area and power consumption. The HVT transistor used in this research is analyzed with different transistor types such as Standard Voltage Threshold (SVT) transistor and Low Voltage Threshold (LVT) transistor. The developed HVT is suitable for low power and less leakage power related applications.

The remaining paper is sorted as follows: Section 2 provides the information about the related works of analog filter and ring oscillator. The detailed information of proposed architecture is given in section 3 whereas the outcomes are provided in the section 4. Lastly, the conclusion is made in section 5.

2. Related work

The information about the existing works of analog filter and ring oscillator are provided in this section.

Lavalle-Aviles and Sánchez-Sinencio [16] presented the Fully Differential (FD) Low-Voltage (LV) fourth-order Butterworth active-RC Analog Low-Pass Filter (ALPF). The ALPF was developed in active-RC topology with the adaptive power, maximum cutoff frequency and programmability. The system level requirements of the filter were achieved by unity-gain frequency, power consumption, feed forward gain-boosting and adjustable output stage. The stabilization was achieved by developing the filter with miller compensation. For a better performance, the filter was required to be utilized with more power.

Osman and Life [17] developed RO-based filters for addressing the process adjustment restriction and linearity of the conventional RO based filters. A linearized current-controlled oscillator (linCCO) was developed to replicate active-RC filter topology's function in phase-domain. The phase and frequency information of an inverter-based RO were extracted by using phase detectors and frequency detectors. The extracted information was used for synthesizing the active filters similar to the integrator-based active-RC filters which were synthesized by resistors and capacitors. The linCCO based filter topology was improved by using a zero compensation technique, but the designed filter achieved worst case bandwidth variations.

Kulej et al. [18] presented voltage, transconductance mode analog filter and quadrature oscillator according to the Differential Difference Transconductance Amplifiers (DDTAs). This analog filter required 2 grounded capacitors and 3 DDTAs. The developed DDTA based filter was offered 5 filtering responses such as band-stop, high-pass, low-pass, band-pass and all-pass responses in a single topology. However, area and frequency of the designed filter were required to be analyzed for this DDTA based filter.

Ozenli et al. [19] developed the Current-Mode (CM) Metal Oxide Semiconductor Field Effect Transistor (MOSFET)-C Analog Filter (AF) for the applications of high frequency band. The cut off frequency of designed CM MOSFET-C AF was changed among 10 and 35 MHz. In high-frequency band, the requirement of baseband filter was obtained by designing a wide tuning range of the CM MOSFET-C AF. However, the degradation at the output was not concentrated on improving the performances of the filter.

Morsali and Shalchian [20] presented the low-power inverter that used a switched pseudocurrent mirror for controlling the pull-up network and minimizing the short-circuit current at transition. The developed inverter created a low-power ring oscillator with aging robustness and enhanced thermal stability. But the developed inverter consumed more area and increased the propagation delay that restricted their utilization in high-density VLSI applications.

Ballo et al. [21] implemented a current-controlled CMOS ring oscillator that used the inverter stage's bulk voltages as controlling terminals for tuning the oscillation frequency. The body-biasing approach was utilized and applied for fixing the inverter to develop low-power low-voltage current-controlled ring oscillator (CCO). The body bias loop was used to eliminate any offset in the input output voltage transfer characteristics. The tuning rate as well as strength against the PVT dissimilarities were improved by cascading the inverter stages. The reduction in leakage current was required to be considered for further reducing the power.

Jo, S.H [22] developed the low-pass analog Infinite Impulse Response (IIR) filter with flat passband to overcome the issue of flatness degradation. An essential sampling frequency was minimized by designing the IIR filter with flat passband that used to minimize the power usage. Additionally, the developed high order IIR filter has higher

degree of freedom over changing input sample weights. The issue of leakage current was not considered while designing the IIR filter.

Martincorena-Arraiza, M et al. [23] presented an enhanced class AB version of Super Source Follower (SSF) for designing the compact and power effective 2nd order ALPF. The utilization of Quasi-Floating Gate (QFG) approach was improved the circuit operation to obtain the significant minimization in power usage and enhance in bandwidth, linearity and pass band gain. The dynamic power consumption was required to be eliminated during the filtering process.

Valencia-Ponce, M.A et al. [24] designed the fractional-order chaotic systems by using three different levels. In first level, the Particle Swarm Optimization (PSO) was used to discover the fractional-orders and coefficients for creating optimum chaotic behavior in the fractional-order Lorenz system. Next, the approximation of fractional-order derivatives was done at the Laplace domain of second level while the CMOS technology was used to design the IC. The fractional-order derivatives were approximated using transfer functions and these fractional-order derivatives were synthesized using active filters which were developed by utilizing the Operational Transconductance Amplifiers (OTAs). The developed OTA was also utilized for designing the adders and subtractors and CMOS 4 quadrant multiplier was used for the multiplication of variables. The partial fraction expansion was used to deal with the issue of high-order polynomials. The power consumption of the designed fractional-order chaotic systems has to be considered for an effective validation.

Castañeda-Aviña, P.R et al. [25] performed the phase noise reduction in the CMOS ring VCO framework. Two different metaheuristics such as Differential Evolution (DE) and PSO were used in ring VCO to minimize the phase noise. The DE and PSO has the capacity for handling the constraints which were appropriate in generating the optimum solutions. The developed ring VCO was mainly concentrated on noise reduction, but it failed to minimize the power consumption.

Jaisawal, R.K et al. [26] used the HVT technique for evaluating the analog/RF and linearity performance of Negative Capacitance Fin Field Effect Transistor (NC-FinFET). The HVT technique was used to minimize the leakage current and enhanced the scaled device's performances. However, the increment in the channel doping of NC-FinFET was increased the channel depletion charge.

Sudhakar, M.V. and Stan, O.P [27] developed the multi-threshold CMOS (MTCMOS) technology which used the transistors with two different threshold voltages such as HVT and LVT. The MTCMOS was included the sleep transistors for boosting the operational speed, minimizing the power usage and minimizing the physical footprint. The increment in the voltage was caused the higher delay of the MTCMOS.

M. Kumngern et al. [28] presented the Low Voltage Mixed Mode (LVMM) 1 V AF which utilized multiple input multiple-output OTAs. The developed filter was utilized 4 OTAs, 1 grounded resistor and 2 grounded capacitors that provides 4 different modes such as current, voltage, transimpedance and transconductance modes. Each mode of function was offered inverting and non-inverting band-stop, high-pass, low-pass, band-pass, and all-pass filter transfer functions. The utilization of folded cascade topology was increased DC voltage gain that maximized the power consumption.

The below Table 1 provides the advantages and limitations of existing approaches.

Table 1. Literature table

Author	Methodology	Advantages	Limitations
Lavalle-Aviles and Sánchez-Sinencio [16]	The FD VL fourth-order Butterworth active-RC ALPF was developed in active-RC topology.	The filter was designed with miller compensation for achieving the stabilization.	The developed ALPF was required to process with more power for enhancing the performance.
Osman and Life [17]	The RO based filter was developed to address the process adjustment restriction and linearity of the conventional RO based filters. The active-RC filter topology's function was replicated using linCCO in the phase-domain.	The usage of zero compensation technique was helped to improve linCCO based filter topology.	However, the developed filter was obtained worst case bandwidth variations.
Kulej et al. [18]	A voltage, transconductance mode analog filter and quadrature oscillator were designed based on DDTA.	In single topology, the developed DDTA based filter was provided 5 filtering responses of band-stop,	The area and frequency of the designed filter were required to be considered while

		high-pass, low-pass, band-pass and all-pass responses.	analyzing the DDTA based filter.
Ozenli et al. [19]	The CM MOSFET-C based analog filter was developed for the applications of high frequency band.	The requirement of baseband filter was achieved by developing a wide tuning range of the CM MOSFET-C AF.	The degradation of the output was required to be concentrated on improving the performances of the filter.
Morsali and Shalchian[20]	The low-power inverter with switched pseudocurrent mirror was developed for controlling the pull-up network and minimizing the short-circuit current at transition.	The developed inverter generated a low-power ring oscillator along with aging robustness and improved the thermal stability.	The inverter utilized more area and increased the propagation delay which limited their usage in high-density VLSI applications.
Ballo et al. [21]	A current-controlled CMOS ring oscillator was developed and it used the inverter stage's bulk voltages as controlling terminals to tune the oscillation frequency.	The offset in the input output voltage transfer characteristics was eliminated using body bias loop.	The leakage current was required to be minimized for further reducing the power consumption.
Jo, S.H [22]	The low-pass analog IIR filter was developed with flat passband to overcome the issue of flatness degradation.	The IIR filter with flat passband was reduced the power usage.	The issue of leakage current was required to be avoided while designing the IIR filter.
Martincorena-Arraiza, M et al. [23]	Enhanced class AB version of SSF was developed for designing the compact and power effective 2nd order ALPF.	The power usage was reduced and bandwidth was enhanced by using QFG approach.	The dynamic power consumption was not eliminated during the filtering process.
Valencia-Ponce, M.A et al. [24]	The fractional-order chaotic systems was designed by using the PSO, approximation of fractional-order derivatives and CMOS technology.	The partial fraction development was used to deal with the issue of high-order polynomials.	The power consumption of the fractional-order chaotic systems was not considered during the validation.
Castañeda-Aviña, P.R et al. [25]	The phase noise reduction was accomplished in the CMOS ring VCO.	The DE and PSO has the ability in handling the constraints that were appropriate in generating the optimum solutions.	The ring VCO was concentrated only on the noise reduction, but it failed to minimize the power consumption.
Jaisawal, R.K et al. [26]	The HVT technique was used for evaluating the analog/RF and linearity of NC-FinFET	The leakage current was reduced and scaled device's performances were enhanced by using the HVT.	The higher channel doping of NC-FinFET was increased the channel depletion charge.
Sudhakar, M.V. and Stan, O.P [27]	MTCMOS technology was developed with two threshold voltages of HVT and LVT.	The incorporation of sleep transistors in MTCMOS was used to enhance the operational speed, reduce the power usage and reduce the physical footprint.	The increment in the input voltage was increased the delay in the MTCMOS.
M. Kumngern et al. [28]	The low power, mixed mode and 1 V AF was developed based on the multiple input multiple-output OTAs	The developed filter was provided the inverting and non-inverting band-stop, high-pass, low-pass, band-pass, and all-pass filter transfer functions.	The power consumption was increased due to the utilization of folded cascade topology.

3. Prototype filter design

The flow of Operational Transconductance Amplifier (OTA) -less 4th order Butterworth low pass filter with proposed architecture is depicted in Fig. 1. This consists of

a cascade of two Tow-Thomas biquads where each biquads is designed using RO integrators. The biquad architectures offers optimum tradeoff among noise, design complexity and linearity than the single loop topology. Moreover, an appropriate biquads ordering is required for achieving highly enhanced results according to the dynamic range and filter's noise performance. The overall design is operated with a supply voltage of 0.9V. A designed low power and low area AF has cascade of proposed 2 Tow-Thomas biquad that is designed by utilizing ring oscillator integrators. The dynamic range in all filters' internal nodes is maximized by using the node phase scaling process. Phase swings that do not cross phase detector's linear scope which are maintained by scaling the charge pump currents and maintained as identical to keep the duty cycles among 0% and 100%.

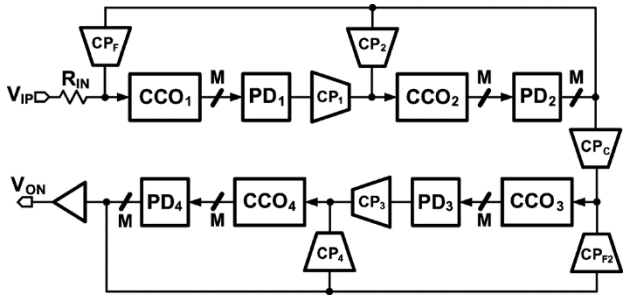

Fig. 1.OTA-less fourth order Butterworth low pass filter with PDTTB architecture

Fig.2 shows the Pseudo-Differential Tow-Thomas Biquad (PDTTB) architecture. The input voltage is transformed into current using resistor R_{IN} and it is reduced from feedback current in a summing node with the input of CCO_1. The resistance is minimized and pole is transferred to input node of CCO_1 for a high frequency by incorporating resistor R_C among the two oscillator inputs. In this architecture, no common-mode current is passed over R_C, while in the differential mode, resistors are set in parallel with resistance of oscillator. Tradeoff among transferring the summing node into high frequency, noise and linearity improvement of Voltage Controlled Oscillator (VCO) are considered for selecting the R_C value. The current flowing level in CCO is minimized due to the feedback current leakage at resistors R_{IN} and R_C. This feedback current leakage based current flowing reduction is displayed as diminished loop gain. In order to overcome this, the first integrator is implemented such that parallel connection of input resistors and resistance in oscillator are similar to the remaining integrators without input resistors.

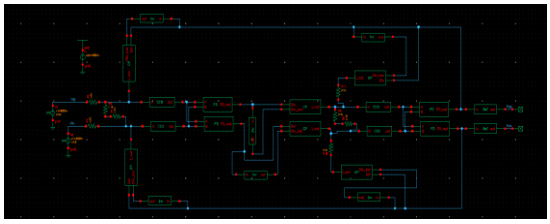

Fig. 2. Design of PDTTB architecture

An adequate selection of charge pump currents is used to design the biquad filter's coefficients. The maximum oscillator input current and gain is determined by accomplishing the transistor-level simulations, once the design of oscillator satisfies the noise requirements. Next, the entire current in every charge pump is achieved by scaling the coefficients of synthesized filter using maximum current. Further, the total current is equally disseminated to each unit branch of the bank. The power of oscillator is scaled along with their noise to filter output. In selected biquad topology, the noise in 2nd integrator is reduced using 1st integrator which leads to reducing the noise. For two pairs of oscillators, the maximum input current is individually discovered because of power scaling.

3.1. Ring Oscillator Design

The gain of Ring oscillator changes according to the process, voltage, and temperature (PVT) that creates the changes in bandwidth of filter. Therefore, Frequency alteration is essential for keeping constant filter bandwidth during the variation in PVT. The tuning process in ring oscillator filters is accomplished in a very linear way via varying bias current, because the time constant of integrator is charge pump gain function K_{CP}. In this proposed architecture, the buffer is incorporated for acquiring the output signal without any degradation. The incorporated buffer is required only for transistors which do not create any impact on overall filter design. The designed ring oscillator generates the analog signal without any input, where Fig. 3 shows the architecture of pseudo-differential ring oscillator. The RO's oscillation frequency is easily tuned by adjusting the size of individual inverters which helps to design the filter with modifiable cutoff frequencies. Moreover, the RO's generally use less power that makes it helpful in energy-efficient systems. The simple architecture of RO leads to minimize the overall area. Here, the output is given as feedback to the input and it is initialized with an overall supply. The ring oscillator has 32 delay stages, each of which are designed by 2 current starved CMOS inverters. Here, the ring oscillator is designed with High Voltage Threshold (HVT) for a better reduction in power consumption. In general, the transistors with HVT present the less subthreshold currents, whereas the transistors with LVT increases the subthreshold currents. The developed HVT is used to minimize the leakage current. Further, this HVT transistor supports in minimizing the standby and dynamic power consumption upto a huge extent without affecting the circuit performance. The outputs of the inverters are connected with feed-forward resistors for supporting the oscillator's differential operation. The topology of feed forward has best noise performances and avoids the contention more than feedback coupling, where the latch and inverter contend and reduce the phase noise. In delay cells, the length of transistor is selected as double the least length, as compromise among rapid fall / rise times and

corner of flicker noise. A number of stages at oscillator are selected to fix minimal VCO gain and obtain a bandwidth of target filter. In oscillator with 64 phases, only 16 phases adequately minimize the Pulse Width Modulated (PWM) tones. In filter, all the four pairs of oscillator utilize the identical length and amount of stages for enhancing the matching. The width of the device at the delay cells of each oscillator is optimized for reducing the noises. For instance, if the 2nd integrator contributed lesser than the first, its delay cells have lesser width.

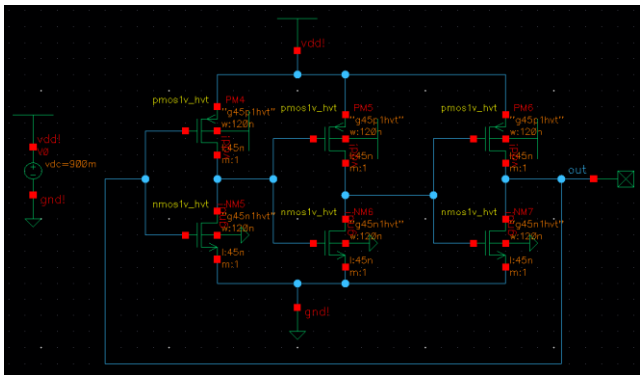

Fig. 3. Design of pseudo-differential ring oscillator

The supply voltage of ring oscillator Vdd is 0.9V and the combination of $PM4\&NM5$, $PM5\&NM6$, and $PM6\&NM7$ are inverters. Consider, the initial input as 0 which makes $PM4$ a closed circuit and $NM5$ an open circuit, therefore the Vdd is passed through $PM4$, and no conduction is done in $NM5$. The $PM4$ is on and $NM5$ is off which generates the output 1, and it is given as input to next pairs of inverters. Subsequently, the pairs of $PM5\&NM6$ returns 0 and $PM6\&NM7$ returns 1. The parameters such as bandwidth, noise, supply voltage and linearity define the selection of center frequency. If the currents of input charge pump are scaled properly, then the high center frequency creates a higher bandwidth. The center frequency of oscillator is fixed by changing the current over the NMOS transistor M_C. The NMOS transistor's source current is utilized to fix the center frequency into minimized area and capacitance that is better than PMOS transistor. In inverter NMOS transistors, the oscillator gain is slightly maximized because of body effect. The delay cell's output swing is lesser than supply voltage and is varied with oscillation's frequency.

The low oscillation frequency requires a huge AC coupling capacitor and 16 level shifters while using the AC-coupled buffers. Accordingly, the incorporation of capacitor and level shifter increases the chip area. The phases are mentioned to supply due to an oscillator function among V_{DD} and V_{CTRL}. Hence, latch is in NMOS and inputs of level shifter in PMOS. An extra NMOS is incorporated in series with latch transistors where it gets connected with the phases of oscillator for improving the performances. The static power consumption is avoided by level shifter when it is operated with less delay. The power consumption (P) of the oscillator is expressed in Eq. (1).

$$P = fMCV^2 (1)$$

Where, oscillation frequency is denoted as f; amount of stages is specified as M; output capacitance of each stage is denoted as C and voltage is denoted as V.

The inverter's output capacitance is charged/ discharged via PMOS and NMOS'son-resistance. Therefore, the oscillation period is proportional to the product of $R_{on}$and C. The capacitance is approximated by C_{ox} that us multiplied by area WL, where W is width and L is length. Accordingly, the on-resistance (R_{on}) shown in Eq. (2) is approximated using square law.

$$R_{on} = \frac{1}{\mu C_{ox}\frac{W}{L}V_{ov}} (2)$$

Where, mobility of charge carriers is denoted as μ and overdrive voltage is V_{ov}.

Further, the oscillation frequency is represented by using Eq. (3).

$$f \propto \frac{1}{MR_{on}C} \propto \frac{\mu V_{ov}}{ML^2} (3)$$

Eqs. (1) and (3) expresses the computation of power consumption and oscillation frequency.

3.2. Phase Detector

The Phase Detector (PD) topology used in this research is two-state PD shown in Fig. 4 which has the linear range of 2π radians. If the error of phase is π radians, then the PD results in 50% duty cycle. The size of developed PD is optimized and it is operated with only 12 transistors which have 2 inputs and one output. The supply voltage given to PD is 0.9V and it has two inputs such as $A\&B$. The truth table of PD is shown in Table 2 which suggests that the PD gives output as 1 when there is a change in phases. The decrement of output cycle lower than 0% creates the duty cycle to 100% or else it creates gross non-linearity. In order to overcome this, the input phase error is guaranteed to never cross the PD's linear range through node phase scaling. The fully symmetric static CMOS logic is used for designing the PD. The nonlinearity created by the internal nodes are extensively minimized by static logic than the dynamic logic.

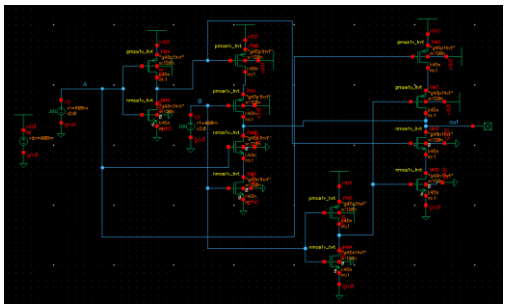

Fig. 4. Design of phase detector

Table 2. Truth table of phase detector

A	B	Output
0	0	0
0	1	1
1	0	1
1	1	0

3.3. Charge Pump

Fig. 5 shows the architecture of charge-pump, where the transistors M_{P1}&M_{N1} refers switches, while M_{P2}&M_{N2} are influenced as current sources. Controlling transistors M_{P1}&M_{N1} along with PD output are used to switch the output current sign. The sudden current source shut off and glitch energy minimization occurs because of switching the transients achieved by incorporating the transistors M_{N2D} and M_{P2D}. The designed charge pump requires the headroom of one overdrive voltage and it has the capacity to operate in low supply voltage. On the other hand, the overdrive voltages of M_{P2} and M_{N2} are maximized for reducing their own noise in high supply voltage.

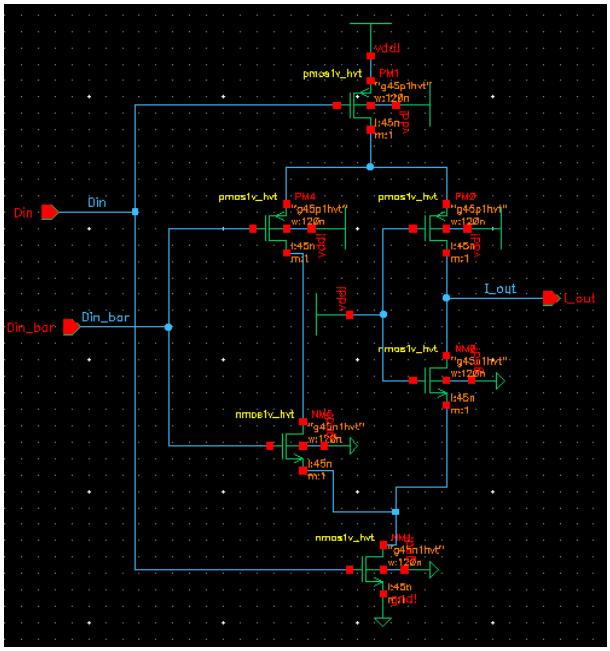

Fig. 5. Design of charge-pump

4. Simulation setup

This section provides the performance analysis of proposed architecture. The proposed architecture is developed for minimizing the power consumption along with the area of the overall filter architecture. The proposed architecture is designed in 45 nm CMOS technology with a supply voltage of 0.9V. Further, the designs are completed and simulated using CADENCE design environment, whereas the system is operated with i5 processor and 8GB RAM. The type of CMOS model used in this research is small signal model. In modern CMOS, the HVT transistors are utilized for achieving the less leakage power. The small signal model is a linear depiction of transistor action around the operating point which utilized for analysing and designing the analog circuits such as amplifiers and filters. This model is important in understanding how changes in the input creates the impact in the output.

The proposed architecture is analyzed using the area, delay, frequency, power and FoM. The reason for choosing these particular metrics are given as follows: Area - The reduction in area minimizes the chip size, cost and enhances the level of integration in CMOS AF; Delay - Reducing the delay supports the filter satisfies the timing requirements and essential for latency sensitive applications; Frequency – Obtaining the required frequency response supports that the filter precisely divides the various frequency bands and it is important in managing the integrity of signal in communication systems; Power – Minimizing the power usage improves the battery life which makes in energy-efficient, and FoM – FoM considers the important parameters of power consumption and frequency which used to define the optimum balance among performance and efficiency.

4.1. Results and discussion

The proposed architecture is analyzed with the output waveform of the Ring oscillator, PD, charge pump and overall circuit. The main objective of this architecture is to minimize the power consumption. The output waveform for ring oscillator is revealed in Fig. 6. The signal in green line is input and the remaining signals are outputs. It depicts that the ring oscillator generates the output based on the feedback signal. The output waveform is represented in red color in Fig. 6, whereas it is individually shown in the Fig. 7.

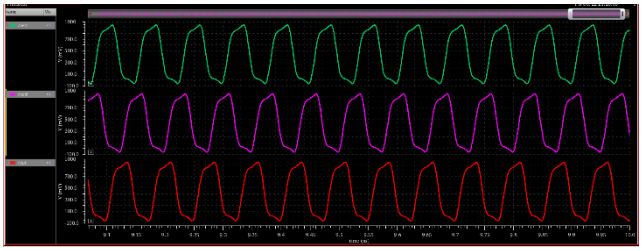

Fig. 6. Input and output waveform of ring oscillator

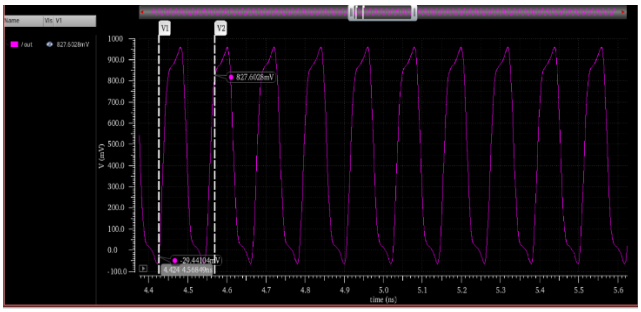

Fig. 7. Output waveform of ring oscillator

From Fig. 7, the frequency of ring oscillator is determined based on the time cycles. Here, one cycle (T) in the waveform is determined based on the following Eq. (4). In general, the frequency is the ratio of 1, and difference between two time cycles i.e., T as expressed in Eq. (5).

$$T = 4.568ns - 4.426ns = 0.142ns \quad (4)$$

$$F = \frac{1}{T} = \frac{1}{0.142\times10^{-9}} = 7.042\ GHz \quad (5)$$

Therefore, the frequency achieved by this oscillator of ring is applied in overall filter architecture is 7.042 GHz. Moreover, consumption of power in ring oscillator is analyzed for two different transistor size configurations along with three types of transistors such as SVT, HVT and LVT. The transistor size configurations are given as follows:

- Case 1: PMOS and NMOS are identical which have a width of 120nm and length of 45nm.
- Case 2: PMOS and NMOS are different to each other. The width and length of PMOS are 300nm and 45nm respectively. Similarly, the width and length of NMOS are 120nm and 45nm respectively.

Tables 3 and 4 shows the power consumption analysis for Case 1 and 2 respectively. From the tables, it is determined that HVT demands less power consumption for both the cases. For example, the power consumption of ring oscillator designed in HVT for case 1 is 6.756 uW, whereas the SVT demands 12.07 uWV, and LVT demands 17.81 uW. The waveform for HVT power and its power consumption computation are shown in the Figs. 8 and 9 respectively. The elimination of leakage current using HVT transistor leads to minimizing the power consumption than the SVT and LVT. Therefore, the overall proposed architecture is designed with HVT transistors for achieving better performances.

Table 3. Analysis of power consumption for Case 1

Transistor type	Power consumption (uW)
SVT	12.07
HVT	6.756
LVT	17.81

Table 4. Analysis of power consumption for Case 2

Transistor type	Power consumption (uW)
SVT	17.72
HVT	9.561
LVT	26.93

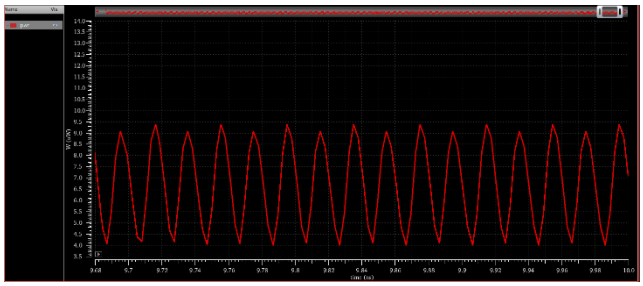

Fig. 8.HVT power waveform

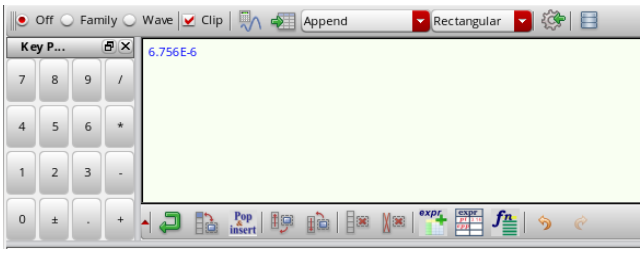

Fig. 9. Computation of HVT power consumption

The phase detector is generally a XOR operation where the size of the transistors are optimized in the overall filter. The output of phase detector is shown in Fig. 10 which has 2 inputs of A&B and one output out. The output is enabled, when the PD detects the phase i.e., variations in the input. For example, the time duration among 2.6 ms to 5.1 ms has different inputs, then it shows the output as 1. Next, the waveform and computation of power for PD is shown in Figs. 11 and 12 respectively. The power consumption of phase detector in the analog filter is 180.8nW.

Fig. 10. Phase detector output

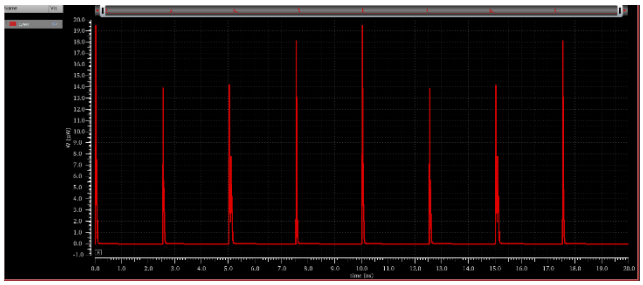

Fig. 11. Power waveform of PD

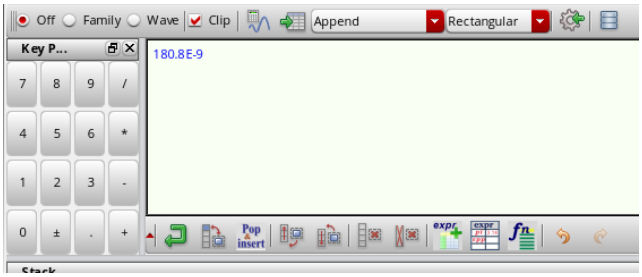

Fig. 12. Computation of phase detector power

The output waveform of pseudo-differential Tow-Thomas biquad architecture is depicted in Fig. 13. There are two inputs given to this proposed architecture such as Vin and Vip, and both are equal to 0.9V. Further, the power waveform and computation of power for PDTTB are shown in Figs. 14 and 15 respectively. The power consumption of overall design is 61.16uW.

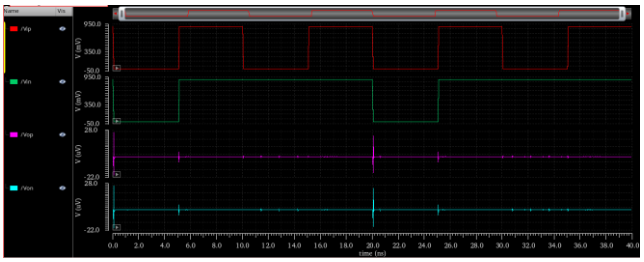

Fig. 13. Output waveform of PDTTB

Table 5 shows the overall architecture performances for the analog filter using PDTTB architecture. After optimizing the architecture of PDTTB based analog filter, a lesser area is obtained which results in less delay and improved frequency. The frequency of 7.042 GHz shows that the developed PDTTB-AF can be used in 5G applications.

Table 5. Performances of overall architecture

Parameter	Value
Area	1237 µm2
Delay	0.142 ns
Frequency	7.042 GHz
Power	61.16µW
FoM	0.0098

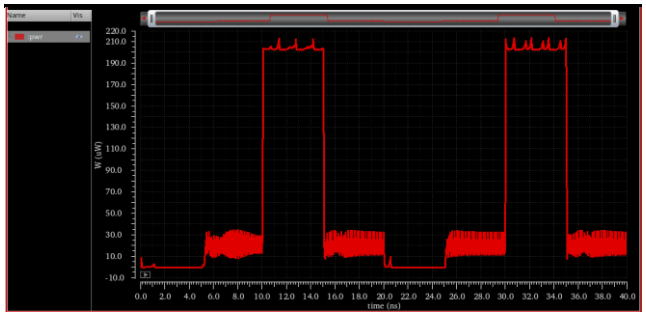

Fig. 14. Power waveform of PDTTB

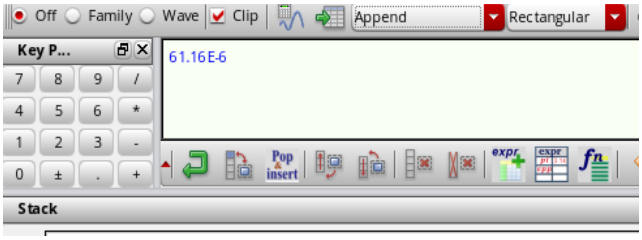

Fig. 15. Power value computation of PDTTB

4.2. Comparative analysis

The comparative analysis of the proposed architecture with existing analog filters is given in this section. The existing filter architecture considered for comparison is LVMM-AF [28]. Table 6 shows the comparison of the proposed with LVMM-AF [28]. From the analysis, it is known that the proposed architecture exhibits better performance than the LVMM-AF [28]. The utilization of HVT in the design of PDTTB is used to minimize the power consumption by avoiding the leakage current.

Table 6. Comparative analysis for proposed architecture

Parameters	LVMM-AF [28]	Proposed
Technology	0.18 µm	45 nm
Power	156.8 µW	61.16 µW

5. Conclusion

In this paper, the PDTTB based analog filter is developed in CMOS 45 technology for filtering process. The buffer is included in the PDTTB architecture to obtain the output signal without any degradation. On the other hand, the power minimization is achieved by using a HVT transistor which helps to lessen the leakage current. The standby and dynamic power consumption is minimized by using the HVT transistor without affecting the circuit performance. The usage of level shifter with significant delay helps to eliminate the static power consumption. According to analysis, proposed PDTTB exhibits better results than the LVMM-AF. The power consumption of PDTTB-AF is 61.16 µW, which is high when compared to the LVMM-AF. In future, power reduction technique can be used for further updating the design of analog filter.

Author Contributions

Ravi Kumar Gali: Conceptualization, RKG and MAR; methodology, VRD; software, MAR; validation, VRD and MAR; formal analysis, MAR;**Venkat Reddy Dasri:**investigation, RKG; resources, MAR; data curation, VRD; writing—original draft preparation, RKG;**M. Asha Rani:**writing—review and editing, MAR; visualization, RKG; supervision, VRD; project administration, MAR

Conflicts of Interest

The authors declare no conflict of interest.

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