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Implementation of Low Speed Dynamic Comparator with Double Tail Cascode Cross-Coupled Pair to Enhance Gain

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Abstract—The dynamic comparator with low performance is designed with a 28 nm CMOS process with a supply voltage of 1.1 V, and is compared to a wide range of double-tail comparator for power consumption and RMS noise with input. Adding a cross-coupling device to I/P differential couple prevents the internal comparison node from being completely unloaded, as opposed to traditional architectures. This reduces power consumption and achieves similar noise levels at the same time. Measurements show that the proposed comparator achieves an input noise of 230 µV. that suppress power reductions by 50%. The proposed circuit consumes 0.198pJ energy per comparison.

Index Terms—*low-noise, Comparator, low-power, double tail latch-type comparator*.

I. Introduction

A comparator is often replaced by comparison with double-sale latches [3] lock is separated by pre-enhancement. This separation allows for independent optimization of circuit offset, noise, speed and performance. With the aim of being Ultralow Performance Applications, the composer plays an important role. The time For inverting configuration

$$V_0 = \begin{cases} V_{0L} & if \quad V_i - V_{REF} > V_{iH} \\ -A_V(V_i - V_{REF}) & if\ V_i \le V_i - V_{REF} \le V_{iH} \\ V_{0H} & if \quad V_i - V_{REF} < V_{iL} \end{cases} \qquad 1$$

Where

Av =The amplification gain

ViL= The low of the input thresholds.

ViH= The high level of the input thresholds.

V0L = The lower of the output thresholds.

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diagram related to this comparison. For each comparison, the node capacitor must be fully ejected from the preamp outputs (INTP and INTN) and be charged to the supply VDD.

Amps can appear using inverter levels allows for increased output quotas for capacitive loads at optimal speeds.

V0H = The higher limits of the output thresholds.

The gain, Av depends on the small voltage difference

$$A_V = \frac{V_{0H} - V_{0L}}{\Delta V} \qquad 2$$

where

$\triangle V$ = the resolution.

If Av = ∞ then

$$ViL = ViH.$$

the signal and output voltage used at the input reaches condition. No frequency compensation was used to reach the multistage comparator.

The current flows through each transistor T1 and T2 are

$$I_{D1} \cong \frac{I_B}{2} + g_{m1}\frac{V_i}{2} \quad 3$$

$$I_{D2} \cong \frac{I_B}{2} - g_{m2}\frac{V_i}{2} \quad 4$$

For the transistor T5 and T6

$$I_{D5} \cong g_{m5}\frac{V_0}{2} \quad 5$$

And

$$I_{D6} \cong g_{m6}\frac{V_0}{2} \quad 6$$

Where

$$V_0 = V_0^+ - V_0^-$$

By replacing the diode connected transistor T3 by its equivalent resistance

$$1/g_{m3} \| 1/g_3$$

In Practice

$$g_{m1} = g_{m2}$$

$$g_{m3} = g_{m4}$$

$$g_{m5} = g_{m6}$$

Based on the small-signal assumption, the current flowing through each of the transistors T1 and T2 are

$$I_{D1} \cong \frac{I_B}{2} + g_{m1}\frac{V_i}{2} \quad 7$$

$$I_{D2} \cong \frac{I_B}{2} - g_{m2}\frac{V_i}{2} \quad 8$$

Where

$$V_i = V_i^+ - V_i^-$$

I_B= Bias Current

By replacing the diode connected transistor T3 by its equivalent resistance

$$1/g_{m3} \| 1/g_3$$

The output voltage expressed as

$$V_0^+ = [1/g_{m3} \| 1/g_3 \| 1/g_1] I_{D3}$$

$$V_0^- = [1/g_{m4} \| 1/g_4 \| 1/g_2] I_{D4}$$

Where

$$I_{D3} = I_{D1} - I_{D6}$$

And

$$I_{D4} = I_{D2} - I_{D5}$$

In Practice

$$g_{m1} = g_{m2}$$

$$g_{m3} = g_{m4}$$

$$g_{m5} = g_{m6}$$

II Proposed work

The proposed comparator architecture is shown in Figure 1. The operational operation of the proposed comparator circuit is explained as follows:

- If transistor M3 is off, there is no direct power current from the soil supply.
- During the amplification phase, when the clock is high, separated from VDD, and M3 provides a drainage path to the ground.
- The gates of M3 and M21 couple to VDD, so node N1 immediately derives into a low voltage where the IR drop is on the switches (M3 and M21).
- The knot P1 works in the same way.
- As soon as the transistors perform M1, M2, M21 and M22 in the linear region.
- During transistor M22 is completely turned off, with transistors M1 and M21 acting as cascode sources is as a defines the gate potential of transistor M21.

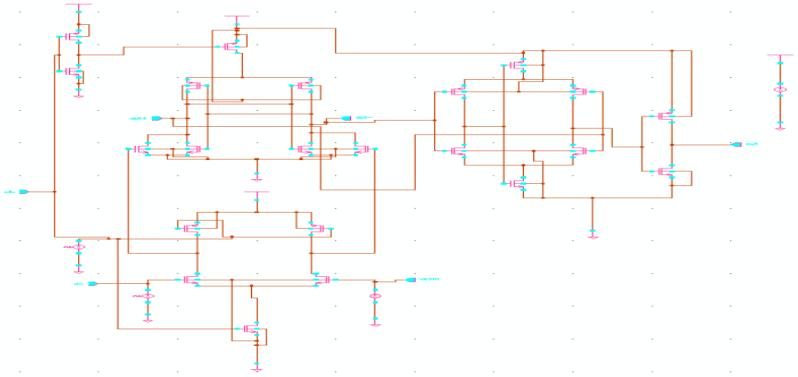

Figure 1: Circuit Diagram of Double Tail Cascode Cross-Coupled dynamic comparator

Figure 1 shows the Double tail dynamic comparator in which circuit comprises of latch stage followed by buffer stage.

III Results and analysis

The sizes of the I/P couples M1 and M2 are kept the same in both designs, and the only additional change to the new cross coupled devices (M21 and M22) to ensure a fair comparison.

For small input difference values, the wide spread of these measurements in the proposed circuit is due to the additional noise produced by M21 and M22. We show parasite-extracted simulation delays in relation to the input differential stress of both the proposed and traditional comparator circuits. . If there is slight difference in input, the proposed circuit will spend more time in the weak inversion area due to the less effectiveness of VGS. This increases the conversion time of the proposed

circuit. Variations in the differential input voltage are measured at a clock speed of 25 MHz Corresponding measurement performance.

Figure 2 shows the DC Analysis of the circuit. Input voltage is taken as 1 V and swept from -1V to +1V. Reference Voltage is taken as 1.2V. From the graph we can conclude that the comparator is working fine.

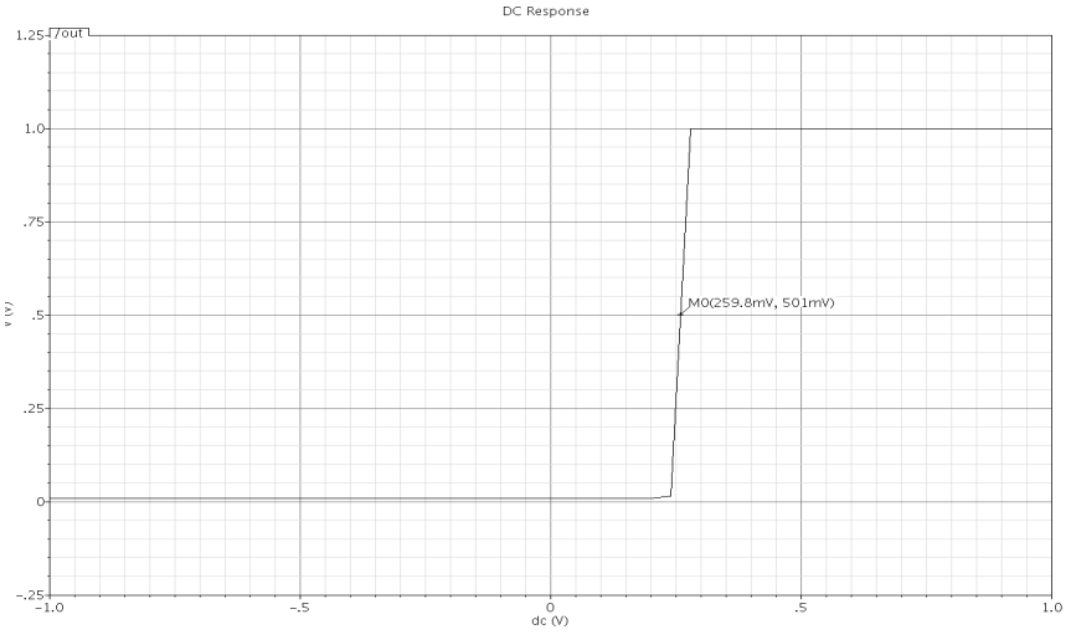

Figure 2: DC analysis of comparator.

Transient Analysis:

Figure 3 shows the transient analysis of the circuit. From this analysis we can say that the output of out+ node in latch stage is affected by noise and fluctuating with the clock transition as that was in the previous comparator. For the transient analysis we have taken pulse voltage source as Input stage and a dc voltage source as reference node.

Figure 3: Transient Analysis of the comparator.

Table I: Results Double Tail Dynamic comparator Cascode Cross-Coupled

Parameter	Before Layout Simulation	After Post Layout Simulation
Offset Voltage	249.8 mV	-
Dynamic Power Dissipation	126.8 µW	144.08 µW
Delay	1.835 nS	2.42 nS
Speed	.570 GHz	.380 GHz
Slew Rate	38.75 V/nS	2.17 V/nS

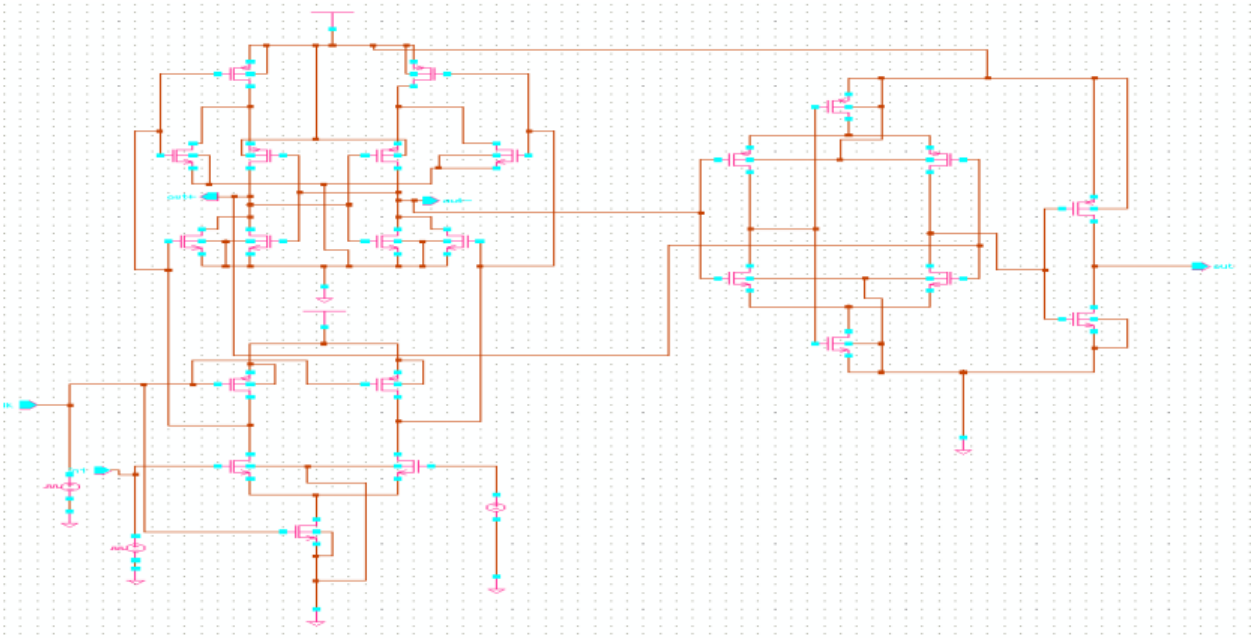

Figure 4: Dynamic Comparator Cascode Cross-Coupled post layout.

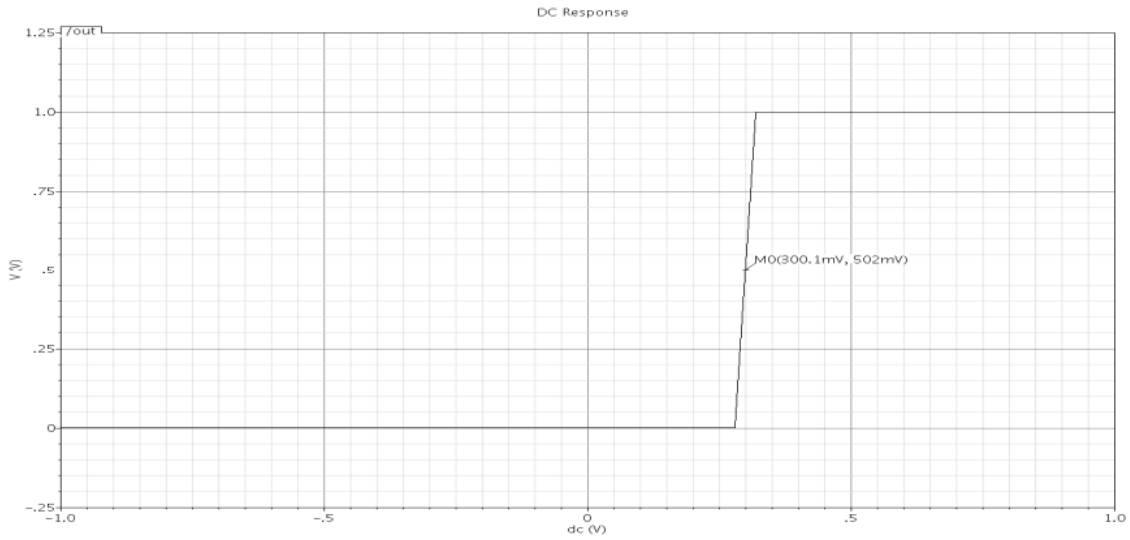

Figure 5: DC Analysis of Dynamic Comparator Cascode Cross-Coupled post layout.

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Figure 5 shows the DC response of the circuit. Input voltage is taken as 1 V and swept from -1V to +1V. Reference Voltage is taken as 1.2V. From the graph we can conclude that the comparator is working fine.

Figure 6 shows the transient analysis of the circuit. From this analysis we can say that the output of out+ node in latch stage is affected by noise and fluctuating with the clock transition as that was in the previous comparator. For the transient analysis we have taken pulse voltage source as Input stage and a dc voltage source as reference node.

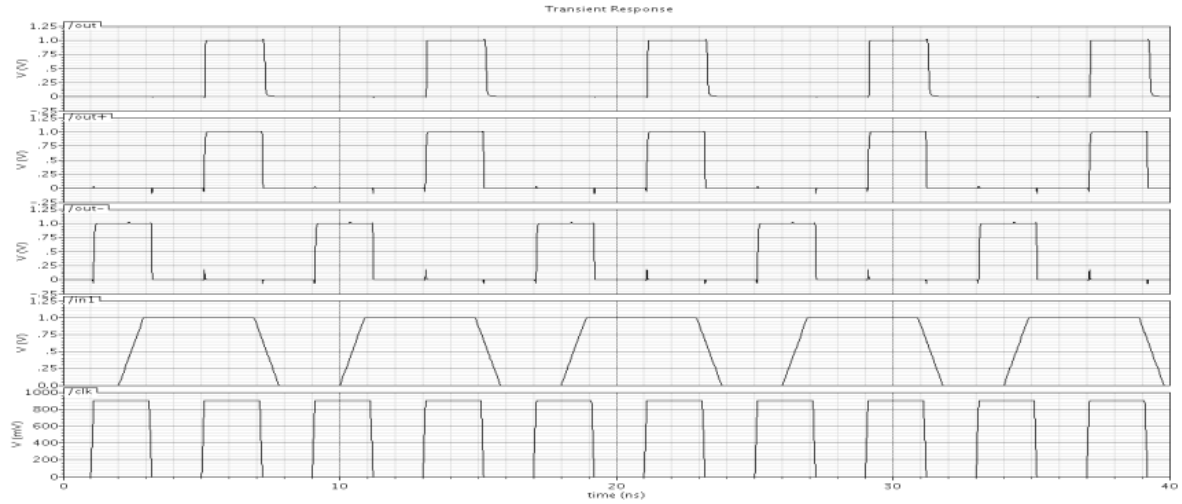

Figure 6: Transient Response of Dynamic Comparator Cascode Cross-Coupled post layout

Table II: Results of Dynamic Comparator without Calibration

Parameter	Before Layout Simulation	After Post Layout Simulation
Offset Voltage	299.1 mV	-
Dynamic Power Dissipation	104.23 µW	111 µW
Delay	60 nS	1.85 nS
Speed	1.539 GHz	.530 GHz
Slew Rate	3.19 V/nS	15.27 V/nS

Analysis of Dynamic Comparator Cascode Cross-Coupled Comparators

Table III: Input Specifications

Technology	**28nm**
Supply Voltage	1.2V
Input Voltage Range	1-2V
Reference voltage	1-1.2V
Clock Frequency	250MHz
Noise	230µVrms
Energy	0.198pJ

Table III summarizes the performance proposed comparator is implemented at a low supply voltage of 1.2V.

IV. Conclusion

The proposed comparator presented here reaches approximately 30% of the measured performance compared to the conventional comparator [4] for similar noise levels. This is achieved by partially unloading the internal comparator node using a simple cross-coupling mechanism. This has provided the architecture with a great design choice in Ultralow Power applications. The proposed circuit is also a low surface solution as it does not require external capacitors or complex logic.

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