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Simulation and Analysis of Non-Inverting and Inverting Mixed Logic 2-4 Decoder

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Abstract: This project involves analysis of Modified Mixed Logic Design abbreviated as MMLD which includes following design logics: Complementary Metal Oxide Semiconductor abbreviated to CMOS logic design, Gate Diffusion Input abbreviated as GDI technique, and Dual Value Logic called as DVL. Two logic styles are used in this paper to reduce power dissipation and delay time are fourteen transistor and fifteen transistor decoders. Every situation requires the use of both regular and inverted decoders. In comparison to conventional CMOS logic design, the suggested decoder provides full swing with a smaller number of transistor count. This suggested MMLD decoder is implemented at multiple frequencies with varied supply voltages using Pyxis Mentor Graphics tool at 45nm with PMOS of width (Wp)=1.4u & length (Lp)=0.35u, NMOS of width (Wn)=1.4u & length (Ln)=0.35u, Fan-out=1, and Wp/Wn=1, which exhibits a reduced power dissipation and delay when compared to other conventional logic design styles.

Keywords: *2:4 Decoder, Modified Mixed Logic Design(MMLD), Gate Diffusion Input(GDI), Dual Value Logic, 45nm Technology*

1. Introduction

In the rapidly evolving landscape of modern electronics, power reduction has emerged as one of the most critical design challenges. As system complexity increases and technology nodes scale down, the demand for low-power, high-performance, and compact electronic systems has intensified. Low-power design is especially vital across a broad range of domains, including integrated circuits (ICs), system-on-chips (SoCs), digital signal processors (DSPs), digital phase-locked loops (DPLLs), and very-large-scale integration (VLSI).

VLSI technology, which enables the integration of thousands to millions of transistors on a single chip, has seen a significant surge in transistor density—approximately 40% annually—as well as an increase in operating frequencies by about 30% per year. These trends, while beneficial for performance, have led to a substantial rise in power consumption and area, making power optimization a top priority in modern chip design.

One of the primary goals of this work is **the simulation and analysis of non-inverting and inverting mixed logic 2-to-4 decoders** with a focus on reducing power consumption. Mixed logic designs offer a promising avenue for minimizing transistor count,thereby lowering power dissipation. Traditional CMOS implementations, although reliable, tend to involve a higher transistor count, leading to increased power usage.

To address this, alternative techniques such as Gate Diffusion Input (GDI), Dual Value Logic (DVL), and Transmission Gate Logic (TGL) have been explored to optimize both transistor efficiency and energy consumption.

- General Procedure
- Overview of 2-4 decoder circuits

A decoder is an essential digital circuit used to convert encoded input signals into distinct output signals. It plays a critical role in applications like memory addressing and data routing in computing systems. Typically, a decoder consists of N input lines and produces 2^n output lines, where each output corresponds to one unique input combination. There are two primary categories of decoders: the non-inverting decoder and the inverting decoder.

In a 2-to-4 non-inverting decoder, two input lines (commonly labelled A and B) determine which one of the four output lines (D0 through D3) is activated. Only one output is set to logic high (1) at any time, while all others remain low (0). The logic functions for the outputs are as follows: D0 = A'B', D1 = A'B, D2 = AB', and D3 = AB. This configuration ensures that each output line corresponds uniquely to one input combination. Such a decoder can be implemented using four NOR gates and two NOT gates.

In contrast, a 2-to-4 inverting decoder operates such that only one output is driven low (0) based on the input values,

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while the remaining outputs stay high (1). The Boolean expressions for the outputs in this case are inverted versions of the non-inverting logic: I0 = (A'B')', I1 = (A'B)', I2 = (AB')', and I3 = (AB)'. A practical implementation of this decoder uses four NAND gates and two NOT gates.

These two types of decoders serve different logical needs in digital circuits, with the non-inverting type used when an active-high output is required, and the inverting type suited for active-low logic systems.

A	B	D0	D1	D2	D3
1	1	0	0	0	1
1	0	0	0	1	0
0	1	0	1	0	0
0	0	1	0	0	0

Tab 1: Logic Table of Non-Inverting 2-4 Decoder

A	B	I0	I1	I2	I3
1	1	1	1	1	0
1	0	1	1	0	1
0	1	1	0	1	1
0	0	0	1	1	1

Tab 2: Logic Table of Inverting 2-4 Decoder

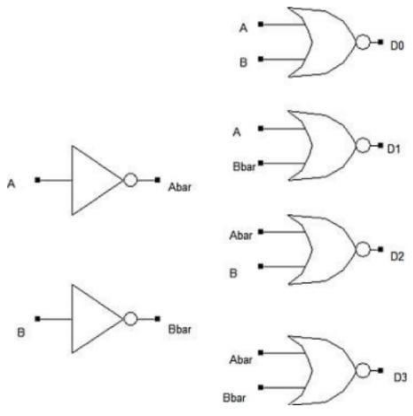

Fig 1: Gate level representation of 2-4 non-inverting decoder

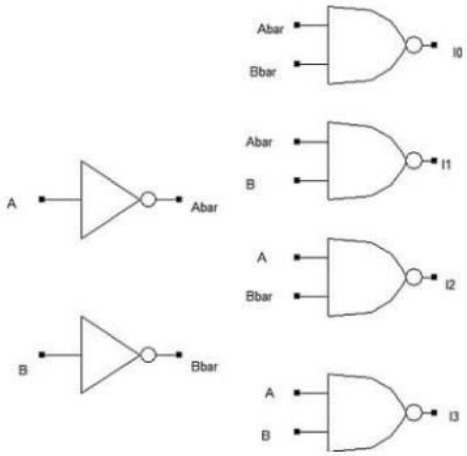

Fig 2: Gate level representation of 2-4 inverting decoder

2. Proposed Method

A.2-4 Decoder using 12T

TGL and DVL make NAND gate and NOR gates simple to implement, which is why they're used in decoders. Take two inputs A and B to make a non-inverting decoder. The D0 and D2 outputs are created using DVL logic design, with signal A acting as a propagating signal. TGL logic design are used for D1 and D3 outputs, as shown in Fig. 3(i). Similarly, 2-to-4 Inverting decoder of outputs I0 and I2 are implemented using TGL logic design, while outputs I1 andI3 are implemented using DVL logic design, as shown in Fig. 3 (ii). Schematic of Non-inverting and Inverting 2-to-4 decoders using TGL and DVL are as shown in Fig.

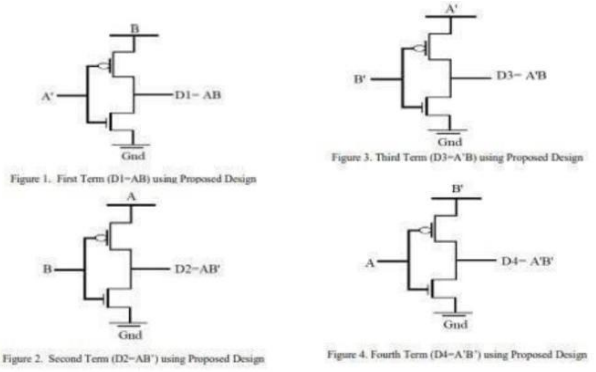

Fig 3(i): Non-inverting 2-4 decoder using 12T

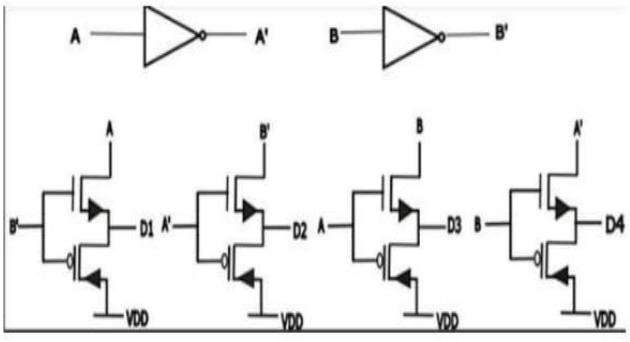

Fig 3(ii): Inverting 2-4 decoder using 12T

Only D0 and D2 are represented using TGL Logic is here, only one Inverting input is considered (A') to reduce extra number of transistor count from inverter converting B to (B'). Consider inputs A and B, where the decoders D0 and D2 outputs are developed using DVL logic design and D1 and D3 outputs are developed using GDI logic design, while the inverter is designed using traditional CMOS logic design is used. As illustrated in Fig. 4, a 2-4 non inverting decoder has seven nFET transistors and five pFET transistors. Maintain the same approach for designing a 2-4 inverting decoder with a twelve transistor architecture with I0 and I2 outputs designed using TGL logic design. As illustrated in Fig 4(ii), the resultant 2-4 inverting decoder with twelve transistors has five nFET transistors and seven pFET transistors. Schematic of Simulation and Analysis of Non-Inverting and Inverting Mixed Logic 2-4 Decoder using twelve transistors are as shown in Fig. 4(i) and 4(ii) respectively.

Schematic Diagram:

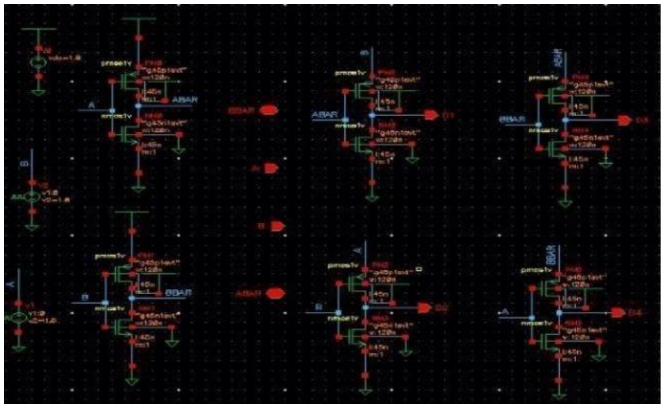

Fig 4(i): schematic diagram of non-inverting 2-4 decoder using 12T

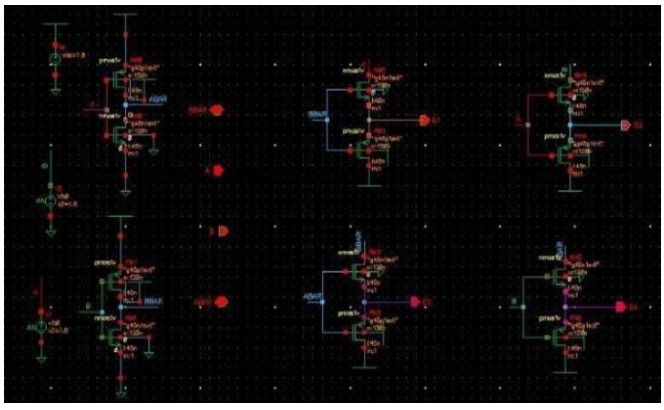

Fig 4(ii): Schematic diagram of inverting 2-4 decoder

3. Application: 4*4 memory using 2-4 decoder

The internal construction of a random-access memory of m words with n bits per word consists of m*n binary storage cells and associated decoding circuits for selecting individual words. The binary cell is the basic building block of a memory unit.

The binary cell has three inputs and one output. The select input enables the cell for reading or writing and the read/write input determines the cell operation when it is selected. A 1 in the read/write input provides the read operation by forming a path from the flip-flop to the output terminal. A 0 in the read/write input provides the write operation by forming a path from the input terminal to the flip-flop

A 4x4 memory design using a 2x4 decoder involves using the decoder to select one of four memory locations and then accessing or storing data in those locations.

Concept

• **Memory Size:** A 4x4 memory means you have 4 locations, and each location holds 4 bits of data. • 2x4 Decoder: A 2x4 decoder takes a 2-bit binary input and produces one of four output lines. Each output line will correspond to one memory location.

• **Memory Storage**: Each memory location in the 4x4 memory array holds 4 bits of data. Therefore, you need 4 storage elements (like flip-flops or registers) for each memory location.

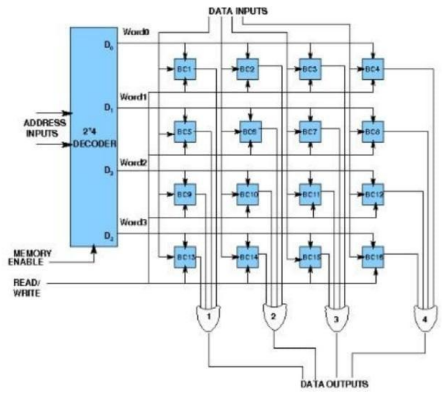

Fig 5(i): Block diagram of 4*4 memory using 2-4 decoder

Schematic diagram of 4*4 memory using 2-4 decoder

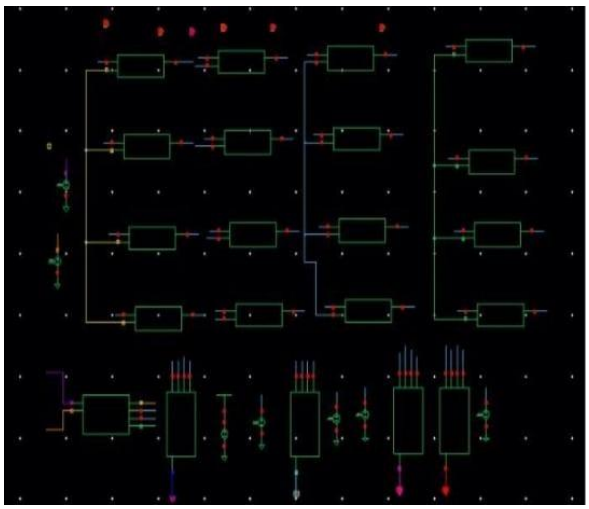

Fig 5(ii): schematic diagram of 4*4 memory using 2-4 decoder

4. Simulations and Results

4.1 Conclusion

This work presents an efficient mixed-logic design methodology for decoder circuits by integrating techniques such as TGL, DVL, and GDI. Utilizing this approach, we have successfully developed both non-inverting and inverting 2-to-4 decoders using only 12 transistors, achieving significant reductions in transistor count and enhanced power-delay performance compared to conventional CMOS implementations. Given that decoders contribute to nearly 30% of total power consumption in memory architectures, optimizing their design is crucial for overall system efficiency. The proposed designs demonstrate notable improvements in speed and power efficiency, making them well-suited for low-power applications. Furthermore, this methodology opens avenues for future work by incorporating additional mixed-logic styles to further optimize performance. These optimized decoders are ideal for applications demanding low power and high performance, such as data multiplexing, seven-segment displays, and memory address decoding.

Waveforms of Non-inverting 2-4 decoder using 12T

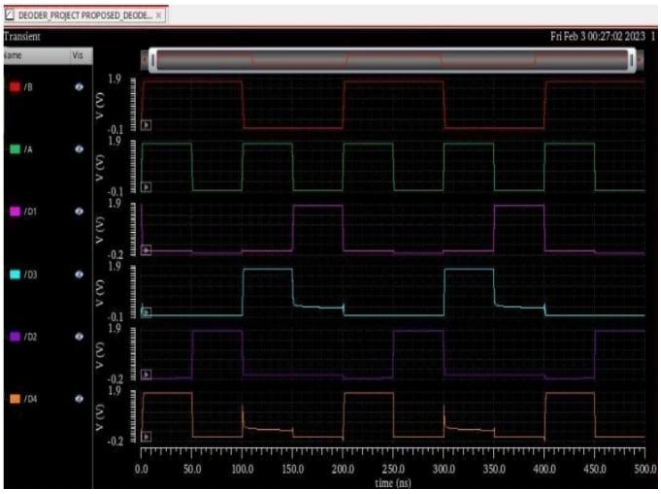

Fig 6(i): waveforms of non inverting 2-4 decoder using 12T

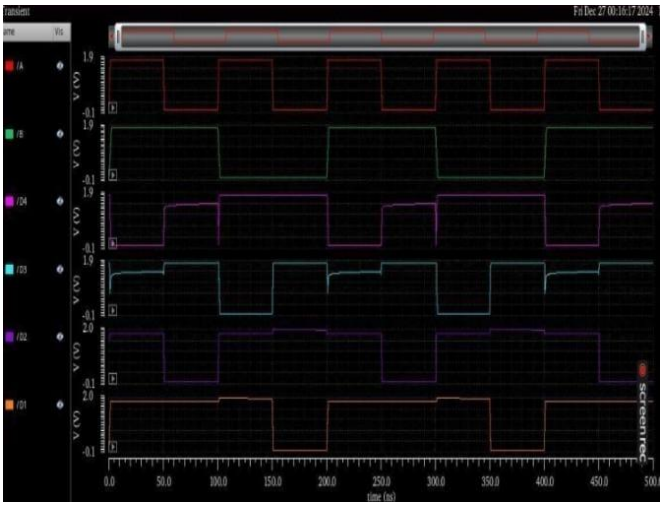

Fig 6(ii): waveform of inverting 2-4 decoder using 12T

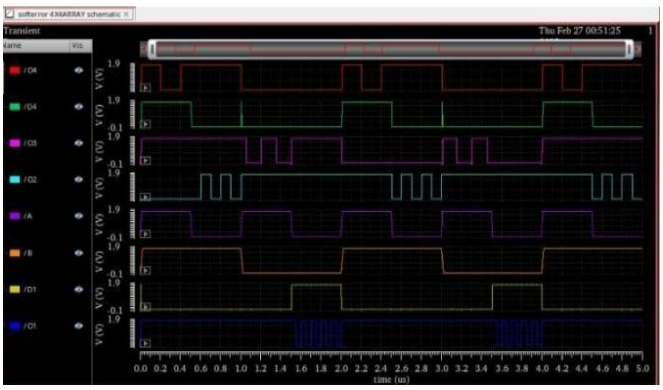

Fig 6(iii): Waveforms of 4*4 memory using 2-4 decoder

Device	Static Power (micro watt)	Dynamic Power (nano watt)	Average Power (nano watt)	Delay (nano sec)
Non-Inverting 12T	103.51	710.88	653.8	50.01
Inverting 12T	94.52	1.43	641.1	50.00
Non-Inverting 14T	153.23	1.0375	509.81	49.98
Inverting 14T	152.62	1.34	530.8	465.9
Non-Inverting 15T	153.3	1.035	572.5	49.98
Inverting 15T	134.08	1.44	16.81	50.00

Tab 3: power dissipation for 2-4 decoders using 12T

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