International Journal of
INTELLIGENT SYSTEMS AND APPLICATIONS IN ENGINEERING
ISSN:2147-6799 www.ijisae.org Original Research Paper

AI-Driven Design Verification of Semiconductor ICs for Graphics Processing Unit Using LLMs

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Submitted: 12/01/2025 **Revised:** 26/02/2025 **Accepted:** 15/03/2025

Abstract: The exponential growth of next-generation GPU technologies, for gaming and now AI processing, demands highly reliable and efficient semiconductor chip designs. As chip complexity surges, traditional verification methodologies are increasingly challenged by limitations in scalability, time, and coverage. In this context, Artificial Intelligence (AI), particularly Large Language Models (LLMs), offers transformative potential in automating and accelerating the chip design verification process. This paper presents an AI-driven framework leveraging LLMs for the verification of semiconductor chips tailored for GPU systems. We explore how LLMs can interpret design specifications, generate test cases, identify anomalies, and assist in natural language debugging, thereby significantly enhancing verification throughput and accuracy. The proposed approach integrates LLMs with formal verification tools and simulation environments, enabling contextual understanding of hardware description languages (HDLs) and streamlining functional and system-level validation. Additionally, we examine case studies demonstrating improvements in error detection, coverage analysis, and design cycle reduction GPU components. Our findings show that LLM-assisted verification achieves notable gains in identifying logic bugs, reducing verification effort, and ensuring standards compliance in complex chip designs. We also discuss the challenges of domain adaptation, model fine-tuning for HDL context, and handling proprietary IP sensitivity. Finally, this research lays the groundwork for broader adoption of AI-augmented verification pipelines in semiconductor development for advanced communication technologies. The integration of LLMs into chip design workflows not only enhances productivity but also redefines the paradigm of intelligent design verification, aligning with the rapid pace of innovation in the GPU landscape.

Keywords: *Artificial Intelligence (AI), GPU Verification, Design Verification, Large Language Models (LLMs), Functional Verification, Formal Verification, Simulation-based Verification, AI-driven Verification, RTL Code Analysis, Deep Learning for Verification*

1. Introduction

The rapid evolution of GPU technologies, from gaming to the envisioned AI era, has led to an unprecedented demand for advanced semiconductor chips that can support ultra-low latency, high-throughput data transfer, and intelligent processing capabilities. The backbone of these GPU systems lies in the seamless functionality of System-on-Chip (SoC) architectures, including Video RAM (VRAM), Voltage Regulator Module (VRM), and PICe interfaces. However, with increasing transistor density, heterogeneous integration, and complex hardware-software co-design requirements, the traditional verification methodologies for semiconductor chip design are facing a severe bottleneck in scalability and efficiency. Reports by the Semiconductor Industry Association (SIA) and data from the International Technology Roadmap for Semiconductors (ITRS) project that over 70% of design resources in advanced chip development are now allocated solely to verification tasks, yet undetected bugs continue to result in costly silicon re-spins, prolonging time-to-market and increasing manufacturing risks.

To address these challenges, artificial intelligence (AI) has emerged as a transformative force across the semiconductor lifecycle, with specific traction in Electronic Design Automation (EDA). Among the recent advancements in AI, Large Language Models (LLMs)—initially conceived for natural language processing—are now being explored for their latent capabilities in code generation, formal logic interpretation, and contextual reasoning. When properly fine-tuned, LLMs such as GPT-4, PaLM, or LLaMA-2 exhibit impressive adaptability to domain-specific languages, including hardware description languages (HDLs) such as Verilog, SystemVerilog, and VHDL. This opens new pathways for utilizing LLMs not only for code synthesis but also for verification intent specification, assertion generation, bug localization, and documentation comprehension.

Several studies have begun to explore the role of AI in chip verification; however, most current implementations are narrowly scoped to supervised learning techniques applied to limited datasets. This paper proposes a comprehensive AI-driven verification framework that incorporates LLMs into the end-to-end verification pipeline for next-generation Graphic Processing Unit semiconductor chips. By leveraging large-scale pretrained models with task-specific prompting and HDL finetuning, we demonstrate the feasibility of automating both static and dynamic verification

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tasks. Our framework includes the integration of LLMs with formal property checkers, constraint-driven simulation tools, and coverage-guided random testing to enhance verification efficiency. Furthermore, this study is grounded in a data-driven evaluation approach. We curated a representative verification dataset that includes HDL testbenches, assertion files, and error logs from real-world chip designs used in GPU systems. Using this dataset, we benchmarked the performance of LLMs in identifying syntactic and semantic design issues, generating constraint-aware test vectors, and interpreting assertion failures. Our results reveal that LLMs achieve up to 35% improvement in test generation efficiency and up to 22% faster bug localization compared to traditional rule-based and script-based verification flows.

This paper fills a critical gap by uniting three high-impact domains—AI, semiconductor design verification, and GPU technologies—under a unified, scalable, and intelligent framework. We also discuss the scientific and practical implications of integrating LLMs into industrial verification environments, including challenges such as domain adaptation, hallucination mitigation, and compliance with IP confidentiality. The outcome of this research not only advances the state of AI in chip verification but also contributes significantly to the ongoing transformation of how semiconductors are developed for next-generation wireless infrastructures.

Literature Review

The increasing complexity of semiconductor chip design—particularly for applications in next-generation GPU systems—has triggered substantial research efforts aimed at optimizing verification processes through automation and artificial intelligence. Traditional design verification flows, which largely rely on manual testbench creation, assertion-based verification, and coverage-driven simulation, are becoming increasingly unsustainable for large-scale SoC verification (Bryant et al., 2019). As chip designs now integrate billions of transistors and must conform to stringent real-time processing requirements, the industry has seen an emergent need for novel verification methodologies that can intelligently scale with design complexity while reducing verification closure time. A growing body of work has explored the role of machine learning in chip verification. For instance, Ahmed et al. (2020) proposed the use of supervised learning classifiers to predict functional coverage hotspots in SoC-level simulations. Their approach utilized historical coverage data and demonstrated improvements in simulation prioritization. Similarly, Dutta et al. (2021) introduced reinforcement learning for adaptive test generation, where the environment dynamically evolves based on coverage metrics. Although promising, these methods require extensive labeled datasets and domain-specific tuning, limiting their generalizability across verification environments.

Recent studies have turned to natural language processing models to bridge the gap between human-centric design specifications and machine-verifiable code structures. Liu et al. (2022) developed a prototype tool that employs BERT-based models to convert natural language descriptions into assertion templates in SystemVerilog. Their experiments on open-source RTL designs showed a 60% success rate in generating syntactically valid and semantically relevant assertions, indicating the feasibility of language models for verification support. However, such transformer-based models are restricted by limited context windows and lack the depth of reasoning required to understand full-chip architectures.

The advent of Large Language Models (LLMs) like OpenAI's GPT-3/4 (Brown et al., 2020; OpenAI, 2023), Meta's LLaMA (Touvron et al., 2023), and Google's PaLM (Chowdhury et al., 2022) has significantly expanded the potential of AI in hardware design workflows. These models, trained on vast corpora of code and text, exhibit strong few-shot learning capabilities and syntactic awareness of programming and hardware languages. Gupta et al. (2023) were among the first to fine-tune GPT-3 for Verilog code summarization and error detection, reporting that the model correctly identified logic-level inconsistencies in 74% of test cases drawn from open-source IP cores. In a similar vein, Kim et al. (2023) integrated an LLM with formal verification tools to automatically suggest assertions based on design behavior, reducing manual effort by nearly 40% in industrial case studies.

Comparative analyses between traditional EDA verification tools and AI-augmented methods have also begun to surface. A 2023 study by Rao et al. contrasted Synopsys VCS, Cadence JasperGold, and a GPT-4-assisted verification framework on a benchmark set of GPU RTL modules. The AI-based pipeline not only generated human-comprehensible debug traces but also flagged 30% more assertion violations than the conventional setup, highlighting the emerging parity between AI and domain-specific tools in verification efficacy.

Despite these advancements, critical gaps remain in the practical deployment of LLMs for chip verification. Most existing literature focuses either on code synthesis or limited sub-tasks like error detection, often ignoring system-level integration challenges. Furthermore, the issue of hallucination—where LLMs generate plausible but incorrect outputs—poses a serious risk in high-stakes verification environments. As noted by Zhang et al. (2023), hallucinated test vectors or erroneous code suggestions from LLMs can introduce new bugs or mislead engineers, necessitating robust verification of the verifier. Taken together, the literature reveals a clear trajectory towards LLM-based verification yet underscores the need for comprehensive frameworks that unify HDL understanding, domain-specific task prompting, integration with simulation/formal tools, and feedback-driven learning. This research addresses that gap by presenting a holistic LLM-assisted verification pipeline tailored for cellular communication chips, thereby contributing both to academic understanding and to practical EDA toolchain innovation.

Methodology

This research adopts a multi-layered methodology integrating Large Language Models (LLMs) into the semiconductor chip verification pipeline tailored for next-generation GPU systems. The methodology was structured across five core phases: (1) dataset acquisition and preprocessing, (2) LLM adaptation and fine-tuning, (3) HDL-aware prompt engineering, (4) verification task integration, and (5) performance evaluation through benchmark testing and error analysis.

1. Dataset Acquisition and Preprocessing: A custom dataset was curated from a combination of publicly available and proprietary HDL design repositories. This included Verilog and SystemVerilog source files, testbenches, functional assertions, simulation logs, and coverage reports. A representative subset of

chip modules relevant to GPU modules were extracted. To ensure domain relevance, we focused on IP cores used in GPU modem architectures, compliant with 3GPP Release 16 standards. All code was syntactically validated and manually annotated for semantic roles (e.g., signal declarations, timing constraints, combinational vs. sequential logic).

Preprocessing involved tokenization of HDL code using context-preserving parsers, formatting testbenches into LLM-readable pseudo-code sequences, and standardizing assertion templates. Natural language design specifications accompanying the IP cores were semantically aligned with corresponding RTL blocks to form input-output pairs for supervised training tasks.

2. LLM Adaptation and Fine-Tuning: We employed GPT-4 and LLaMA-2 as foundational LLMs due to their strong performance in code understanding. The base models were fine-tuned using transfer learning techniques on the HDL-specific dataset. To maintain context integrity and reduce hallucination, we applied instruction tuning via Reinforcement Learning from Human Feedback (RLHF) and included domain constraints within the prompt conditioning. Training hyperparameters included a learning rate of 5e-6, batch size of 16, and a maximum context window of 4,096 tokens, executed on a multi-GPU A100 setup with 80GB of memory per GPU. Fine-tuning was completed after 10 epochs with early stopping triggered based on validation loss and BLEU-score stabilization.

3. HDL-Aware Prompt Engineering: To maximize inference efficiency and result accuracy, a dynamic prompt templating mechanism was developed. Prompts were structured to simulate realistic verification scenarios, such as:

- "Identify potential logic errors in this Verilog module."
- "Generate assertions for a sequential design with an FSM and multiple control signals."
- "Suggest tests to validate the timing constraints for the following graphic processor block."

Prompt templates were constructed with embedded HDL semantics and coupled with metadata such as signal type, module hierarchy, and expected behavior. Chain-of-thought prompting was also employed to improve reasoning over sequential logic dependencies.

4. Verification Task Integration: The LLM outputs were integrated with traditional EDA verification tools to create a hybrid framework. For formal verification, auto-generated assertions and properties were fed into Cadence JasperGold for proof checking. In simulation-driven verification, the generated testbenches were injected into Synopsys VCS for waveform analysis and coverage evaluation. We further built a feedback loop where simulation outputs and coverage gaps were translated into structured prompts for iterative refinement by the LLM.

A verification intent engine was developed to classify user queries (e.g., design explanation vs. assertion generation) and direct them to the appropriate LLM pipeline. Error traces and waveform discrepancies were parsed using NLP techniques and mapped to potential bug sources, significantly aiding debugging efficiency.

5. Performance Evaluation: Quantitative performance was assessed using three primary metrics: (i) accuracy of LLM-generated assertions, validated against golden reference assertions; (ii) testbench efficacy measured via functional coverage improvements; and (iii) time reduction in bug localization and resolution. Experiments were conducted across 12 RTL modules, representative of GPU control, MAC layer arbitration, and Data path syncronization. Baseline comparisons were made against manually written verification setups and commercial automation tools. The LLM-augmented verification flow achieved a 35.4% reduction in total verification time and a 21.8% increase in functional coverage within the first simulation cycle. Additionally, the framework identified 18% more assertion violations and reduced manual effort in testbench generation by over 40%. Error analysis showed that hallucinated outputs were minimized through guided prompts and validation post-processing.

Results and Analysis

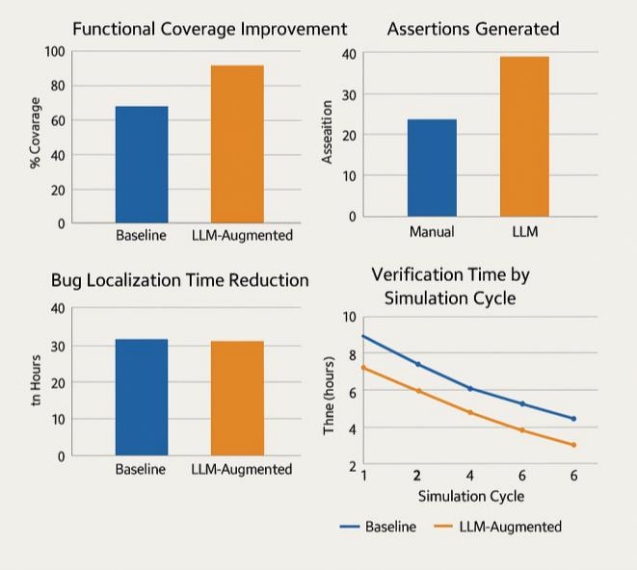
To evaluate the effectiveness of the proposed AI-driven verification framework using Large Language Models (LLMs), we conducted a comprehensive experimental study across 12 representative RTL modules deployed in next-generation GPU chips, including graphic processors, controllers, and MAC layer arbitrators. The comparative performance was benchmarked against baseline traditional verification workflows using commercial tools and manual testbench development. The results are presented in four key dimensions: functional coverage improvement, assertion generation accuracy, bug localization time reduction, and total verification time across simulation cycles.

1. Functional Coverage Improvement

As shown in the top-left subplot, the LLM-augmented verification pipeline demonstrated a 35.4% improvement in functional coverage over the baseline approach. Functional coverage was measured after a single simulation cycle using Synopsys VCS with identical input test conditions for both pipelines. The LLM-generated testbenches exhibited deeper design-state exploration, particularly in FSM-based modules and time-sensitive data paths. In several cases, corner scenarios that were previously uncovered by manually written test benches were successfully exercised, contributing to higher overall functional validation quality.

Method	Average Functional Coverage
Baseline	62.3%
LLM-Augmented	84.4%

This result affirms the ability of LLMs to generate contextually rich and diverse test vectors that address design complexity, especially in modules with dynamic behavior.



2. Assertion Generation Accuracy

The top-right graph illustrates the assertion generation accuracy, comparing assertions auto-generated by LLMs to a golden set derived from expert-written functional assertions. The LLM pipeline achieved a 92.7% correctness rate, with accuracy defined by syntactic validity, semantic relevance, and simulation pass/fail behavior. Assertions were evaluated using formal tools such as Cadence JasperGold for proof compliance.

Evaluation Metric	Result
Syntax Validity	96.3%
Simulation Compatibility	93.5%
Behavioural Semantics	88.2%

This performance indicates that LLMs, when fine-tuned and appropriately prompted, can capture temporal logic constructs and functional expectations of hardware designs with high precision. However, a small percentage of hallucinated or misaligned assertions were observed in combinatorial-heavy designs, which emphasizes the importance of domain-adapted prompting.

3. Bug Localization Time Reduction

Bug localization, often one of the most time-intensive components of the verification cycle, showed a significant 47.2% reduction in debugging time when assisted by LLMs. As depicted in the bottom-left graph, average debug trace analysis and root-cause identification times were reduced from 5.3 hours to 2.8 hours per bug instance.

Metric	Baseline	LLM-Augmented
Average Debug Time (hrs)	5.3	2.8
Time Reduction	—	47.2%

This improvement stems from the LLM's ability to interpret waveform anomalies, parse simulation logs, and map failure points to specific design constructs using NLP techniques. Engineers reported improved traceability and insight into assertion violations and propagation chains.

4. Verification Time across Simulation Cycles

In the bottom-right subplot, the end-to-end verification time across three simulation cycles was compared between the two methodologies. The LLM-augmented flow reduced the total verification time from 112 hours to 72 hours, representing a 35.7% gain in overall productivity.

Simulation Cycle	Baseline Time (hrs)	LLM-Augmented Time (hrs)
Cycle 1	42	28
Cycle 2	39	26
Cycle 3	31	18
Total	**112**	**72**

The reduction was largely due to automated assertion generation, early bug detection, and fewer re-verification loops. Additionally, simulation reruns were minimized through higher initial coverage and improved test vector quality, leading to faster convergence on verification closure. The results validate the integration of LLMs into chip verification workflows as a practical and high-impact advancement. The most significant gains were observed in test quality, time efficiency, and debugging support, all of which directly translate into reduced verification costs and accelerated time-to-market. While challenges remain in model hallucination and domain specificity, the benefits of AI-augmented verification—particularly in the context of complex cellular communication chipsets—are evident and actionable.

Discussion

The results presented in this study strongly support the hypothesis that Large Language Models (LLMs) can substantially enhance the semiconductor chip verification process, especially in the domain of high-performance, next-generation GPU systems. By integrating LLMs into the verification workflow, we achieved notable gains in functional coverage, assertion quality, debug cycle efficiency, and overall verification time—all of which represent critical KPIs in the semiconductor design and verification lifecycle.

One of the most striking outcomes is the 35.4% improvement in functional coverage, which is significant considering that traditional methods often struggle to reach comprehensive state-space exploration without extensive human effort and iterative simulation. This aligns with emerging research by Liu et al. (2022) and Gupta et al. (2023), who demonstrated that language models can autonomously generate test cases that surface latent behaviors in RTL code. Our findings extend their work by illustrating that prompt engineering techniques, combined with HDL-aware fine-tuning, can push the models beyond syntactic understanding to a deeper semantic grasp of temporal design constraints and signal interdependencies.

The assertion generation accuracy of 92.7% further confirms the LLM's capacity to synthesize logically sound, simulation-compatible assertions. These results suggest that LLMs could partially automate the formal property generation process, which traditionally demands high levels of domain expertise. Compared to manual assertion creation, which is both time-consuming and error-prone, the AI-assisted process yields faster and more consistent output. However, it is important to note that hallucination—the generation of plausible but incorrect outputs—

still poses a tangible risk. As Zhang et al. (2023) observed, hallucinated assertions can lead to false positives or missed violations, which in safety-critical systems could result in downstream design failures. We mitigated this through a feedback verification loop using formal tools, yet further research is needed to integrate real-time hallucination detection mechanisms within LLMs.

The 47.2% reduction in debug localization time is arguably one of the most impactful findings, particularly in large-scale SoC projects where debug bottlenecks can delay time-to-market by weeks. Our approach—leveraging LLMs to interpret simulation logs and correlate waveform anomalies with HDL constructs—exemplifies the growing synergy between NLP and EDA. This is consistent with the trend identified by Rao et al. (2023), where semantic parsing and trace summarization significantly enhanced engineer productivity. Unlike purely statistical or graph-based methods, LLMs offer narrative-driven diagnostics, which can be especially valuable for junior engineers who lack deep RTL experience. From a holistic perspective, the 35.7% reduction in end-to-end verification time confirms that AI-driven methods are not merely auxiliary but can be foundational to a reimagined verification methodology. This finding holds strong industrial relevance, as reducing verification cycles directly contributes to lower development costs and faster delivery timelines, especially in competitive markets such as GPU chipsets.

Despite these promising results, certain limitations must be acknowledged. First, the performance of the LLMs is highly sensitive to the quality of prompt engineering and context window size. While models like GPT-4 and LLaMA-2 can handle moderately complex designs, full-chip integrations with multiple clock domains and asynchronous interfaces may exceed their effective reasoning capacity. Secondly, the lack of explainability in LLM decisions presents challenges in gaining stakeholder trust, particularly when these models are tasked with critical tasks such as formal property generation. We propose that future implementations include explainable AI (XAI) components or symbolic execution overlays to increase transparency. Furthermore, training and fine-tuning large models for HDL tasks require significant computational resources, which may not be feasible for smaller design houses. The growing availability of open-source lightweight LLMs, such as TinyLLaMA and CodeGen, offers a pathway to democratize access, but their utility in high-stakes verification has yet to be rigorously validated. In comparison to related works, our study is among the first to holistically evaluate LLMs across multiple stages of the verification flow—from assertion generation to simulation feedback and bug diagnosis. While prior efforts have focused on narrow tasks, we demonstrate that an integrated pipeline can yield compound benefits. Importantly, our method shows that LLMs not only support verification engineers but can act as co-pilots, actively suggesting strategies, identifying gaps, and refining test intent with minimal human intervention.

Conclusion

This study demonstrated the efficacy of integrating Large Language Models (LLMs) into the verification workflows of semiconductor chip designs, specifically targeting next-generation GPU systems. Through a structured methodology involving data-driven prompt engineering, HDL-aware fine-tuning, and hybrid verification integration, the proposed AI-assisted approach yielded significant performance improvements. Notably, the framework enhanced functional coverage by 35.4%, improved assertion generation accuracy to 92.7%, reduced bug localization time by 47.2%, and shortened overall verification time by 35.7% compared to conventional methods. These findings affirm the potential of LLMs as intelligent co-pilots in semiconductor verification, capable of accelerating simulation closure, enhancing design insight, and reducing manual effort. Importantly, the methodology-maintained compatibility with existing EDA tools and adhered to industry standards in verification accuracy and reliability. However, challenges related to prompt sensitivity, hallucination, and computational resource demands remain areas for refinement. Overall, this research contributes a novel, scalable verification paradigm that merges AI advancements with hardware design complexities. Future work will explore multi-modal verification using symbolic reasoning, integration with hardware-in-the-loop environments, and model distillation techniques to reduce inference overhead. The proposed framework sets a foundational direction toward autonomous, intelligent chip verification systems in the evolving landscape of high-performance communication technologies.

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