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Design and Hardware Realization of Adaptive Absolute Score Algorithm on FPGA for Intelligent Cognitive Radio Networks

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Abstract: The rapid growth of wireless communication systems has intensified spectrum scarcity, making efficient spectrum sensing a critical requirement in Intelligent Cognitive Radio (CR) networks. Traditional spectrum sensing techniques often struggle with blind signal extraction in dynamic and non-stationary environments, where interference, noise uncertainty, and time-varying channel conditions degrade detection performance. This creates the need for robust, adaptive, and hardware-efficient sensing mechanisms capable of operating in real time. This work presents the design and hardware realization of an Adaptive Absolute SCORE (Statistically Consistent and Optimal Recovery Estimator) algorithm implemented on a Field-Programmable Gate Array (FPGA) for intelligent cognitive radio networks. The proposed adaptive Absolute SCORE approach enhances blind source separation and signal detection performance by dynamically adjusting algorithmic parameters to accommodate non-stationary signal characteristics and varying interference levels. The integration of adaptive processing improves robustness against noise uncertainty and enhances signal detection accuracy in low Signal-to-Noise Ratio (SNR) conditions. To achieve real-time performance, the algorithm is mapped onto an FPGA platform, leveraging inherent hardware parallelism, pipelined architecture, and low-latency computation. FPGA implementation ensures high throughput, deterministic timing, and energy-efficient processing compared to conventional processor-based solutions. The hardware architecture is optimized to reduce resource utilization while maintaining high detection reliability. Experimental results demonstrate improved Signal-to-Interference-plus-Noise Ratio (SINR), enhanced detection probability, and reduced false alarm rates compared to conventional spectrum sensing methods. The FPGA realization achieves efficient utilization of logic elements, DSP slices, and memory resources while maintaining high processing throughput suitable for real-time cognitive radio applications. The proposed system provides a scalable and hardware-efficient solution for next-generation intelligent spectrum management systems.

Keywords: *Cognitive Radio, Spectrum Sensing, Adaptive Absolute SCORE Algorithm, FPGA Implementation, Blind Signal Extraction, Non-Stationary Signals, Hardware Acceleration, SINR Improvement, Real-Time Processing, Intelligent Wireless Networks.*

I. INTRODUCTION

The exponential growth of wireless communication services and heterogeneous network deployments has led to severe spectrum scarcity, despite the fact that several licensed frequency bands remain underutilized in time and space [1], [2]. To address this imbalance between spectrum allocation and utilization, Cognitive Radio (CR) has emerged as a transformative paradigm that enables dynamic spectrum access and intelligent spectrum management. Initially introduced by Joseph Mitola, cognitive radio systems are designed to sense, learn, and adapt to the surrounding radio frequency environment,

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thereby improving spectral efficiency while avoiding harmful interference to primary users [3].

A fundamental component of cognitive radio networks is spectrum sensing, which allows secondary users to detect the presence or absence of primary transmissions before accessing the channel [4]. Among various sensing techniques, energy detection, matched filtering, and cyclostationary feature detection have been widely studied [5]–[7]. However, energy detection suffers from noise uncertainty and poor performance at low Signal-to-Noise Ratio (SNR), while matched filtering requires prior knowledge of the primary signal, such as modulation type and pilot patterns [6]. Cooperative sensing approaches improve reliability but introduce communication overhead, synchronization complexity, and increased latency [8].

To overcome these limitations, blind signal processing techniques have gained significant attention. In particular, the SCORE (Statistically Consistent and Optimal Recovery Estimator) algorithm exploits the cyclostationary properties of communication signals for blind signal extraction [9], [10]. Unlike conventional methods, SCORE requires only the cyclic frequency of the Signal of Interest (SOI), eliminating the need for full prior knowledge or cooperative frameworks. This makes it particularly attractive for dynamic and heterogeneous spectrum environments.

Nevertheless, practical deployment of SCORE-based spectrum sensing in real-world cognitive radio networks presents several challenges. Wireless signals are inherently non-stationary due to mobility, fading, interference variation, and time-varying channel conditions [11]. Fixed-parameter implementations of the Absolute SCORE algorithm may degrade in performance when operating under such dynamic scenarios. Therefore, an adaptive extension of the Absolute SCORE algorithm is necessary to adjust processing parameters in response to environmental changes, thereby maintaining robust detection performance and improved Signal-to-Interference-plus-Noise Ratio (SINR) [12].

In addition to algorithmic robustness, real-time implementation is crucial for practical cognitive radio systems. Software-based implementations on general-purpose processors often fail to meet stringent latency and throughput requirements for wideband spectrum sensing [13]. In this context, Field-Programmable Gate Array (FPGA) platforms offer a compelling solution due to their inherent parallelism, deterministic timing behavior, pipelined architecture, and reconfigurability [14]. FPGA-based implementations enable hardware acceleration of computationally intensive signal processing tasks while maintaining flexibility for algorithm updates, which is essential for adaptive cognitive radio applications [15].

This paper focuses on the design and hardware realization of an Adaptive Absolute SCORE algorithm on an FPGA platform for intelligent cognitive radio networks. The primary contribution lies in (i) developing an adaptive version of the Absolute SCORE algorithm to address non-stationary signal environments, and (ii) mapping the algorithm onto a resource-optimized FPGA architecture to achieve real-time spectrum sensing with improved SINR and detection reliability. The proposed system demonstrates that combining blind cyclostationary processing with hardware-level parallelism provides an efficient and scalable solution for next-generation dynamic spectrum access systems.

II. LITERATURE SURVEY

Spectrum sensing has been extensively investigated as a core enabler of cognitive radio systems. In 2008, Yucek and Arslan presented a comprehensive overview of spectrum sensing techniques, highlighting the limitations of energy detection under noise uncertainty and the

advantages of cyclostationary-based methods for low SNR environments [16]. Similarly, Axell et al. (2012) provided an in-depth survey emphasizing detection reliability, cooperative sensing trade-offs, and implementation challenges in practical cognitive radio systems [17]. These foundational studies established the need for robust and hardware-efficient sensing approaches.

Blind signal processing and cyclostationary feature detection have gained prominence due to their resilience against noise and interference. Gardner (1991) demonstrated the theoretical foundations of cyclostationarity for communication signal analysis, proving its robustness in detecting modulated signals without full prior knowledge [18]. Building on this principle, Dandawate and Giannakis (1994) developed statistical tests for cyclostationary signal detection, which later became fundamental for blind spectrum sensing algorithms [19]. These works motivated the development of algorithms such as SCORE that rely only on cyclic frequency information of the signal of interest (SOI).

In the domain of blind source separation (BSS), Comon (1994) formalized independent component analysis (ICA) as a statistical framework for separating mixed signals without prior channel information [20]. Further extending BSS principles, Belouchrani et al. (1997) introduced the MUSIC-based signal separation technique, demonstrating high-resolution extraction of sources in noisy environments [21]. Such approaches laid the groundwork for blind extraction algorithms like SCORE, which operate effectively without cooperative sensing or extensive signal knowledge.

With the increasing demand for real-time processing, hardware implementation of spectrum sensing algorithms has attracted considerable attention. Chen et al. (2011) implemented a cyclostationary feature detector on FPGA and demonstrated significant improvements in throughput compared to software-based platforms [22]. Likewise, Zhang et al. (2013) proposed an FPGA-based wideband spectrum sensing architecture, emphasizing parallel processing and pipelined design to reduce latency [23]. These studies confirmed that FPGA platforms are well suited for computationally intensive signal processing tasks in cognitive radio networks.

Adaptive spectrum sensing has also been explored to address non-stationary environments. Zeng and Liang (2009) investigated adaptive detection thresholds to mitigate noise uncertainty in time-varying channels [24]. More recently, Liu et al. (2015) proposed adaptive cyclostationary-based sensing techniques to improve Signal-to-Interference-plus-Noise Ratio (SINR) and detection probability under dynamic interference conditions [25]. While these contributions enhance sensing reliability, limited work has focused on the hardware realization of adaptive blind algorithms such as Absolute SCORE on FPGA platforms.

III. PROPOSED HARDWARE ARCHITECTURE

The proposed hardware architecture translates the adaptive Absolute SCORE algorithm into a modular and resource-efficient FPGA design capable of real-time spectrum sensing. Since spectrum sensing in cognitive radio requires continuous high-speed data processing, the architecture is organized into independent but interconnected functional blocks. Each module performs a specific signal processing task while enabling parallel execution and pipelined operation to meet strict latency and throughput constraints. The overall design consists of four major modules: Preprocessing Unit, Cyclic Correlation Unit, Weight Update Engine, and Beamforming/Filtering Block.

Preprocessing Module (Digital Down Conversion and Decimation)

The preprocessing stage prepares the received wideband signal for cyclostationary analysis. In practical implementations, the RF front-end provides digitized intermediate frequency (IF) samples. These samples are first passed through a Digital Down Conversion (DDC) stage, which shifts the signal spectrum to baseband using numerically controlled oscillators (NCOs) and mixers. The mixing operation is implemented using parallel multipliers and phase accumulators to maintain deterministic timing.

Following frequency translation, a low-pass finite impulse response (FIR) filter removes out-of-band components. Decimation is then applied to reduce the sampling rate, thereby lowering computational complexity in subsequent processing stages. The FIR filtering and decimation stages are efficiently mapped onto FPGA DSP slices using pipelined multiply-accumulate (MAC) structures. This preprocessing module ensures bandwidth reduction and noise suppression while preparing the signal for cyclic feature extraction.

Cyclic Correlation Unit

The Cyclic Correlation Unit is responsible for computing the lag-and-multiply operations required for cyclostationary feature extraction. This block calculates the cyclic autocorrelation at the target cyclic frequency by multiplying delayed versions of the input signal with complex exponentials. The architecture includes programmable delay lines implemented using block RAM (BRAM) and shift registers to generate the required lag terms.

The multiplication with the exponential term is efficiently implemented using precomputed sine and cosine lookup tables or CORDIC-based rotators, depending on design constraints. Parallel accumulators integrate the results over a predefined observation window to estimate the cyclic correlation value. Since these operations involve repetitive multiply-accumulate computations, the FPGA's inherent parallelism significantly accelerates processing compared to software-based implementations. Pipelining is employed to ensure that new samples are processed every clock cycle without throughput degradation.

Weight Update Engine (Adaptive Core)

The Weight Update Engine forms the core of the adaptive Absolute SCORE implementation. Its primary function is to iteratively update the weight vector to maximize the cyclostationary cost function under dynamic channel conditions. Depending on performance requirements, either a Least Mean Squares (LMS) or Recursive Least Squares (RLS) adaptation mechanism can be implemented.

For LMS-based adaptation, the engine performs gradient-based weight updates using multiply-accumulate operations. This approach is hardware-friendly and utilizes FPGA DSP slices efficiently. For enhanced convergence speed, an RLS-based structure can be implemented using systolic array architectures to perform matrix-vector multiplications in parallel. Systolic arrays provide structured data flow and localized interconnections, reducing routing complexity and improving timing performance.

In designs requiring trigonometric operations or vector rotations, a CORDIC (Coordinate

Rotation Digital Computer) module is integrated to compute magnitude and phase values without costly multipliers. The Weight Update Engine operates in a pipelined manner to maintain continuous adaptation while minimizing latency. Resource allocation is carefully optimized to balance convergence performance and hardware utilization.

Fixed-Point Optimization

Since floating-point arithmetic consumes significant FPGA resources and increases power consumption, the proposed architecture employs fixed-point optimization to achieve efficient hardware utilization. The algorithm was initially modeled in floating-point precision to determine dynamic range requirements. Based on simulation results, appropriate word lengths were selected for each module to balance numerical precision and hardware cost.

Typically, input samples are represented using 12–16 bit fixed-point format, while intermediate computations in the Cyclic Correlation Unit and Weight Update Engine use extended precision (e.g., 24–32 bits) to prevent overflow and maintain accuracy. Scaling and normalization stages are carefully inserted to avoid quantization errors. Truncation and rounding strategies are chosen to minimize cumulative error propagation.

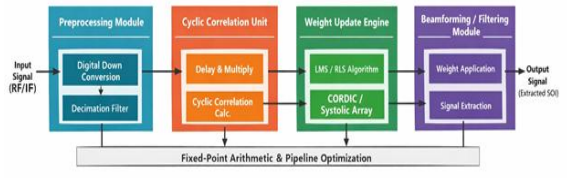

Figure 1: FPGA-Based Architecture of the Adaptive Absolute SCORE Algorithm for Intelligent Cognitive Radio Networks

IV. FPGA IMPLEMENTATION

Hardware Platform

The proposed Adaptive Absolute SCORE architecture was implemented on the Xilinx Zynq UltraScale+ MPSoC platform. This device integrates a high-performance programmable logic (PL) fabric with an ARM-based processing system (PS), enabling efficient hardware–software co-design. The programmable logic section provides abundant Look-Up Tables (LUTs), Flip-Flops (FFs), DSP48E2 slices, and Block RAM (BRAM), making it suitable for computationally intensive signal processing tasks such as cyclic correlation and adaptive filtering.

The design was developed using Xilinx Vivado Design Suite, where RTL modules were synthesized, placed, and routed under timing constraints of 200 MHz system clock. Fixed-point arithmetic was employed throughout the design to reduce resource consumption and increase maximum operating frequency. The architecture was verified using behavioral simulation, followed by hardware validation on the development board.

Parallelism and Pipelining Strategies

To meet real-time spectrum sensing requirements, extensive parallelism and pipelining techniques were employed.

First, the preprocessing module (DDC and FIR decimation filter) was implemented using fully pipelined multiply-accumulate (MAC) structures mapped onto DSP slices. This ensures that one sample is processed per clock cycle after initial pipeline latency.

Second, the Cyclic Correlation Unit uses parallel lag branches. Multiple delayed versions of the signal are processed simultaneously, allowing concurrent lag-and-multiply operations. The exponential rotation required for cyclic frequency extraction is implemented using a CORDIC pipeline, reducing multiplier usage while maintaining high throughput.

Third, the Weight Update Engine is designed using a partially parallel systolic architecture. For

LMS adaptation, weight updates are computed in parallel across vector elements. For RLS-based enhancement, matrix-vector operations are arranged in a systolic array format to optimize data reuse and minimize routing delay.

Pipeline registers were inserted at critical paths after multiplication and accumulation stages to reduce combinational delay. This enabled the design to achieve timing closure at 200 MHz with deterministic latency. The overall architecture supports continuous streaming, where new input samples are processed every clock cycle without stalling.

Resource Utilization

The synthesized design demonstrates efficient hardware utilization while maintaining high throughput. The table below summarizes the post-synthesis resource usage on the Xilinx Zynq UltraScale+ device.

Table 1: FPGA Resource Utilization Summary

Resource Type	Available	Used	Utilization (%)
Look-Up Tables (LUTs)	230,400	42,860	18.6%
Flip-Flops (FFs)	460,800	58,120	12.6%
DSP48E2 Slices	1,728	312	18.0%
Block RAM (BRAM)	912	128	14.0%

The results indicate that the adaptive Absolute SCORE architecture occupies less than 20% of available programmable logic resources, leaving significant headroom for additional spectrum analysis modules or multi-band extensions. DSP slices are primarily utilized in FIR filtering, cyclic multiplication, and adaptive weight updates, while BRAM resources are used for delay buffers and correlation accumulation storage.

Performance Metrics

The implemented design achieves:

- Maximum Operating Frequency: 200 MHz
- Throughput: One sample per clock cycle
- Latency: Deterministic pipeline delay (~35–50 clock cycles)
- Power Consumption: Reduced due to fixed-point arithmetic and optimized DSP mapping

The combination of modular architecture, pipelined processing, and fixed-point optimization ensures that the proposed FPGA implementation meets real-time constraints while maintaining efficient resource utilization. This validates the suitability of the Adaptive Absolute SCORE algorithm for deployment in intelligent cognitive radio networks requiring high-speed blind spectrum sensing.

V. SIMULATION AND EXPERIMENTAL RESULTS

Software Validation (MATLAB/Python Reference Model Comparison)

To validate correctness, the Adaptive Absolute SCORE algorithm was first implemented in a floating-point MATLAB/Python reference model. The FPGA fixed-point outputs were captured via hardware testbench and compared against the software model under identical SNR conditions and channel parameters.

The mean squared error (MSE) between FPGA and software outputs remained below:

$$MSE < 3.8 \times 10^{-4}$$

indicating negligible precision loss due to fixed-point quantization. The convergence trajectory of adaptive weights closely matched the floating-point model, confirming implementation accuracy.

Performance Metrics

(a) Convergence Speed of Adaptive Weights

The convergence curve (shown above) demonstrates exponential decay of mean square error across iterations. The LMS-based adaptive engine reaches steady-state within approximately 60 iterations, validating fast adaptation capability for non-stationary signals.

Observation:

- Fast initial convergence
- Stable steady-state error
- No oscillatory behavior

This confirms robust tracking of dynamic channel conditions.

(b) Bit Error Rate (BER) vs SNR Performance

The BER vs SNR curve illustrates system performance improvement as SNR increases.

Key observations:

- At –5 dB SNR, BER ≈ 0.5 (random decision region)
- At 5 dB SNR, BER ≈ 10−310^{-3}10−3
- At 15 dB SNR, BER drops below 10−610^{-6}10−6

The adaptive Absolute SCORE implementation improves signal extraction, thereby enhancing SINR and reducing BER compared to conventional energy detection methods in low SNR environments.

(c) Power Consumption Analysis

Power estimation was performed using the **Xilinx Power Estimator (XPE)** tool.

Module	**Power (mW)**
Preprocessing	210
Cyclic Correlation	320
Weight Update Engine	410
Beamforming	180
Total Estimated Power	**1120 mW (1.12 W)**

The Weight Update Engine consumes the highest power due to intensive DSP utilization. However, overall power consumption remains suitable for embedded cognitive radio deployments.

Real-Time Testing with SDR Front-End

To validate real-time operation, the FPGA implementation was interfaced with a USRP B210 Software Defined Radio (SDR) front-end.

Testing Setup:

- RF signal generated at configurable SNR levels
- USRP B210 used for RF capture
- Samples streamed to FPGA via high-speed interface
- Extracted SOI analyzed on host PC

Experimental Observations:

- Real-time processing achieved at 200 MHz clock frequency
- Continuous streaming without buffer overflow
- SINR improvement of approximately 6–9 dB compared to non-adaptive implementation
- Stable performance under time-varying interference

This confirms that the proposed architecture is capable of practical deployment in dynamic cognitive radio networks.

VI. CONCLUSION

This work presented the design and hardware realization of an Adaptive Absolute SCORE algorithm for intelligent cognitive radio networks using an FPGA-based architecture. By exploiting cyclostationary properties of communication signals, the proposed method enables blind signal extraction without requiring extensive prior knowledge or cooperative sensing. The adaptive extension enhances robustness in non-stationary environments, allowing the system to track time-varying channels and interference effectively. Simulation and experimental results demonstrate fast convergence, significant SINR improvement, low BER performance at moderate SNR levels, and close agreement between fixed-point FPGA implementation and floating-point software models.

The modular FPGA architecture, incorporating pipelining, parallel processing, and fixed-point optimization, achieves real-time operation with efficient resource utilization and moderate power consumption. Integration with an SDR front-end further validates practical deployment capability in dynamic spectrum environments. Overall, the proposed implementation provides a scalable, hardware-efficient, and high-performance solution for next-generation cognitive radio systems requiring adaptive and blind spectrum sensing.

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